Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 324-325

D-6-3

# 65nm Node Transistor Characteristic Evaluation Technology for Assembly Stress and Assembly Stress Relaxation Design

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**Abstract**

We have first developed a new method to evaluate the effects of assembly stresses on transistor characteristics with a test chip fabricated by 65nm technology with low-k films. As the test chip is composed of a transistor matrix array under probing/bonding pads, we can obtain the distribution map of characteristic fluctuations caused by assembly stresses. Using this method, we have found the stacked via guard structure has stress relaxation effects to reduce Ids fluctuations less than about 30%.

**Introduction**

Recently, the chip shrinking has been speeding up and then the number of pad has been increased to integrate as SOC chips. A small chip with many pads requires the probing/bonding pads placed on transistors. For realizing the pads on transistors, it's most important to suppress the fluctuations of transistor characteristics caused by assembly processes, such as probing, wire bonding, plastic molding, etc. A basic method to evaluate the fluctuations of resistance and mobility due to external stresses using piezoresistive elements have been reported [1,2]. A conventional evaluation results for the variation of transistor characteristics in a chip or a wafer have also been reported [3,4]. But there are no reports for the effects of assembly processes on transistor characteristics fluctuations with their distribution map.

As for 65nm node LSI chips with low-k-based multi-interconnects, it has been found that the transistor performance is quite sensitive to assembly stress. In this work, we have first developed a new method to evaluate the effect of assembly stresses using a unique test chip composed of 65nm process technology, and resultantly we have proposed the stress relaxation structure suited for 65nm node and beyond.

**Transistor Characteristic Evaluation Technology for Assembly Stress**

To evaluate transistor characteristic fluctuations caused by assembly processes with reasonable accuracy, the test chip has been newly developed by 65nm technology (Table1). The microphotograph of the test chip is shown in Fig.1. The test chip has matrix array of transistors. Using decoder circuits similar to those of memory devices, each transistor can be measured respectively. In order to make sure the effect of probing for pads on transistor structure, probing pads are placed on the transistor array as shown in Fig.2. The transistor pitch is decided to detect the peak position of probing. As clearly shown in Fig.3, we have successfully obtained ⊿Ids ((Ids before probing－Ids during probing)/ Ids before probing) distribution map by measuring Ids before and during probing with this chip. Figs.4 and 5 show the distribution of ⊿Ids along the probe direction for N and P channel transistors. The distribution profiles are quite different between N-channel and P-channel. Considering from the previous report [2] that ⊿Ids of N- channel may be influenced mainly by the vertical stresses and ⊿Ids of P-channel by horizontal stresses, it has been first observed that the stress distribution of this probe, that is, the vertical stress is located at position A (probe point) in N channel, and horizontal pull stress at position B, horizontal push stress at position C, respectively.

**Assembly Stress Relaxation Design**

The test chips have some kinds of structure for pads on transistor array and their schematic cross sections are shown in Figs.6-8. We have evaluated and compared normalized ⊿Ids values among these structures (Fig.9).

A. Stacked metals pad structure

⊿Ids for Al/Cu stacked metals pad (A1) is bigger than that for Al/SiN/Cu isolated metals pad (A2). (10.5% for Nch and 14.5% for Pch). From this result, it is found that SiN layer sandwiched between metals has a stress relaxation effect.

B. Via-guard structure

The via-guard structure (B2) has stacked vias surrounding the transistors and large area metal (Cu) plates above transistors. A no-guard structure (B1) has no vias and no metals between aluminum pad and transistors. The results show B2 structure can reduce the probing stress to transistor because of the assembly stress concentrations on vias. (12.2% for Nch and 9.3% for Pch).

C. Via structure on transistors

We designed three kinds of patterns: stacked vias (C1), zigzag vias (C2) and no vias (C3) as reference above transistors. The results show that zigzag vias and stacked vias bring larger stresses than no vias. (10.7% for Nch and 6.6% for Pch).

Fig.10 shows the combined results of each result mentioned above A, B and C. The combination of via-guard structure (B2), AL/SiN/Cu pad (A2) and no via structure on transistors (C3) was most acceptable, and has an excellent relaxation effect (Nch 30.9% and Pch 25.3%) compared to worst case (A1+B1+C1).

**Conclusions**

We have developed the transistor characteristic evaluation technology for assembly stress on 65nm node test chips. ⊿Ids distribution and actual direction of probing stress for N and P channels have been observed for the first time.

From viewpoint of assembly stress relaxation, it has been found that the combined structure of via-guard structure (B2), AL/SiN/Cu pad and no via structure was most excellent with less than about 30% of relaxation effect.

**References**

[1] Charles S. Smith, Physical Review, vol.94 p.43, 1954.
[2] Arthur T. Bradley, et al., IEEE Transactions on Electron Devices, vol.48 p.2009, 2001.
[3] T. Mizuno, et al., IEEE Transactions on Electron Devices, vol.41 p.2216, 1994.
[4] N. Izumi, et al., IEEE Transactions on Semiconductor Manufacturing, vol.17 p.248, 2004.

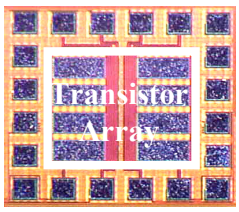


Fig.1 Microphotograph of the test chip.

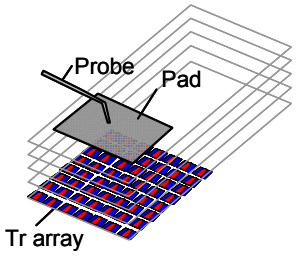


Fig.2 Schematic illustration of transistor array structure.

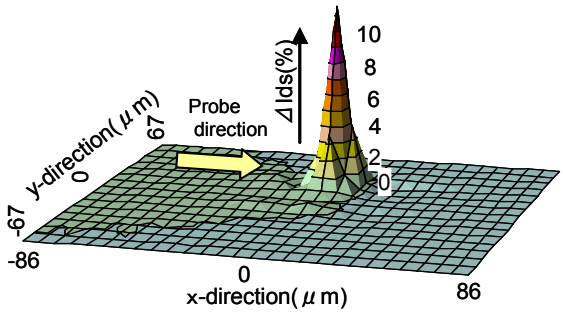


Fig.3 ⊿Ids distribution mapping during probing.

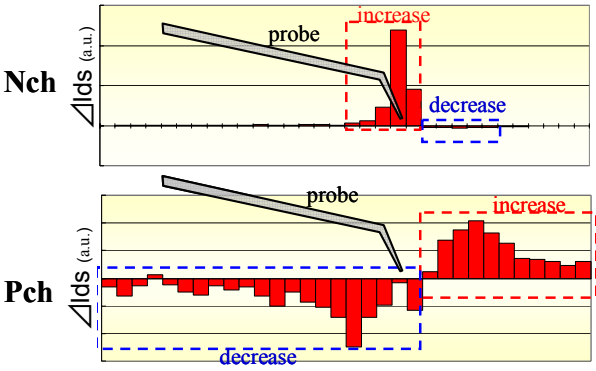


Fig.4 Distribution of ⊿Ids along the probe direction (Nch,Pch).

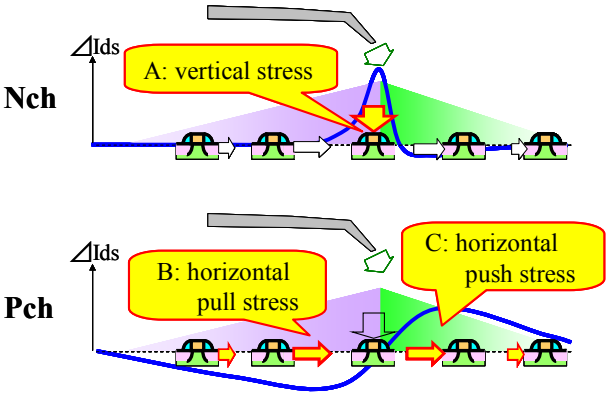


Fig.5 Probing stress mechanism presumption (Nch,Pch).

**A. Stacked metals pad structure**

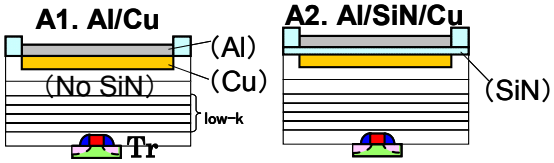


Fig.6 Schematic illustration of stacked metals pad structure.

**B.Via-guard structure**

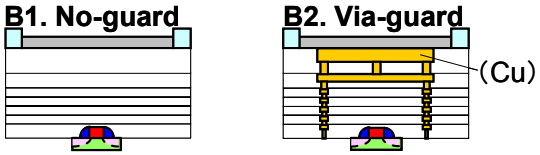


Fig.7 Schematic illustration of via-guard structure.

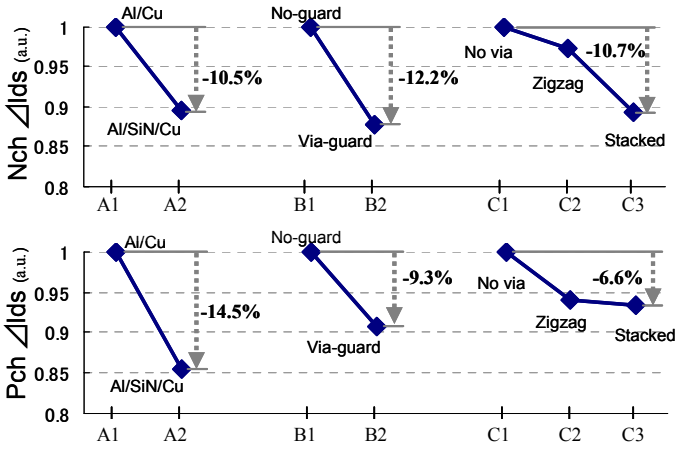


Fig.9 ⊿Ids peak of various structures.

**C.Via structure**

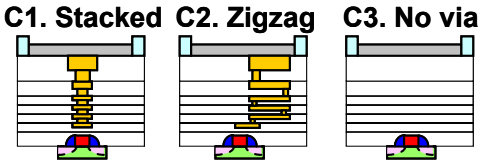


Fig.8 Schematic illustration of via structure.

Table 1 Process features

| | |
|---|---|
| Technology | 65nm CMOS<br>M1:180nm,M2:200nm,low-k |
| Metal Wire | 7-8Metal (Cu) |
| Pad Metal | Al |
| Voltage | 1.2V, 3.3V |

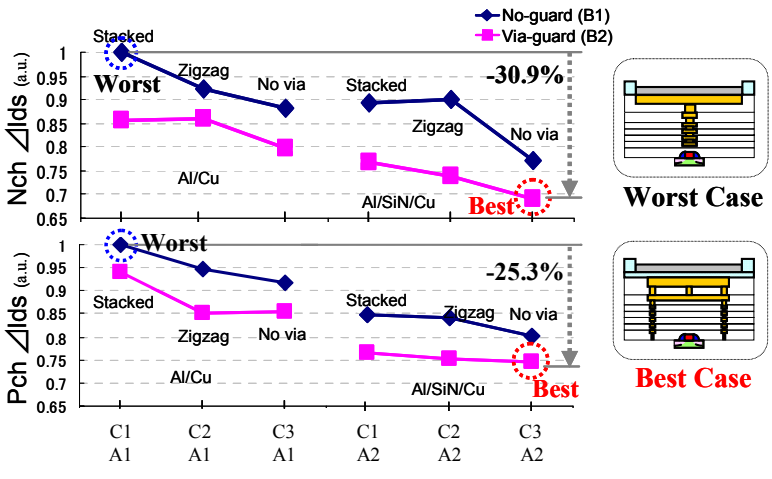


Fig.10 ⊿Ids peak of various combination structures.