Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 914-915

D-7-4

Analysis of hole trapping into pentacene FET by Optical Second Harmonic Generation and C-V measurements

Eunju Lim, Takaaki Manaka, Ryosuke Tamura, Mitsumasa Iwamoto

Department of Physical Electronics, Tokyo Institute of Technology,
2-12-1 O-okayama, Meguro-ku, Tokyo 152-8552, Japan
*e-mail: iwamoto@pe.titech.ac.jp

1. Introduction

Over the past decade, a great deal of research has been focused on the development of organic material electronics. Especially, organic thin film transistor (OTFT) devices are intensively studied for the practical use such as smart cards, identification tags and flexible displays [1]. Pentacene is one of the materials used for OTFTs that shows most excellent semiconducting performance, and much experimental effort, such as modification of the film quality, has been made to improve the device performance [2]. In order to drive the field effect transistor (FET), we need to apply high drain-source voltage V_{ds} and gate voltage V_g different from that of Si-FETs [1]. Therefore, to achieve high organic FET (OFET) devices efficiency, we need to fully understand at least the following three key processes, i.e., carrier injection, carrier accumulation and carrier transport, in combination with the FET characteristics. It has been pointed out that carrier injection from source and drain electrodes makes a dominant contribution to the pentacene FETs operation [3]. It was revealed that the charge carriers forming the conducting channel of pentacene FETs are mainly holes injected from the source electrode by means of the optical second harmonic generation (SHG) measurement as well as the capacitance-voltage (C-V) measurements [4]. Taking into account these, we successfully employed a Maxwell-Wagner (MW) model for analyzing the current-voltage (I-V) and C-V characteristics of FETs, without knowledge of semiconductor physics [3]. The successful employment of dielectrics physics for analyzing the organic FETs motivated us to study the hysteresis behaviors observed in the FET characteristics of OFETs, because the hysteresis effect is one of the most important issues to be clarified for the use of organic devices. By using the electric field induced second harmonic generation (EFISHG) and C-V measurements, we could show the originates from holes that are injected from the source electrode and subsequently trapped in pentacene layer. Further, we discussed how the hysteresis behavior links to the FET characteristics that can be explained using a MW model.

2. Experimental

The FET has a top-contact structure with the pentacene material deposited. Prior to the deposition of the pentacene active layer, the SiO_2 gate insulator was chemically treated by adopting UV/ozone-octadecyltri-chlorosilane($C_{18}H_{37}SiCl_{13}$) (OTS) treatment. After the treatment, pentacene was deposited by thermal evaporation method at a pressure less than 10^{-4} Pa. The substrate temperature was kept about 350 K during the deposition and the deposition rate was fixed at 0.4 Å/sec. The channel length (L) and width (W) were 50 μm and 1.5 mm, respectively, and electrode is deposited to Au. In SHG measurement, using the reflect optical geometry, fundamental light was focused on the channel region of the OFET using an objective lens (f= 150 mm) and the spot size was approximately 20 μm^2. The light source was an optical parametric oscillator (OPO: Continuum Surelite OPO) pumped by the third-harmonic light of a Q-switched Nd-YAG laser (Continuum: SureliteII-10). Wavelength was fixed at 1120 nm. The SH light from the sample was detected by a photomultiplier tube (Hamamatsu photonics: type-R955).

3. Results and Discussion

To further clarify the hysteresis behavior, the C-V measurement was carried out. Figure 1 shows the C-V characteristics of a 100-nm thickness pentacene FET using an UV/ozone-OTS treated substrate. The measurement was carried out with an a.c. frequency of 100 Hz in the region between V_{gs} = -40 and +40 V, after

biasing the sample at a voltage of -40 V for 10 min. The hysteresis behavior was seen between forward and backward scans sweep direction. In Figure, we plotted the capacitance corresponding to the capacitance without channel formation, 4.7×10^{-11} F. The capacitance increases and saturates at a voltage around -40 V due to the channel formation [3]. We may consider that holes are injected from the source electrode and subsequently trapped at the interface between pentacene/SiO_2 interface, and they are origins of trapped carriers.

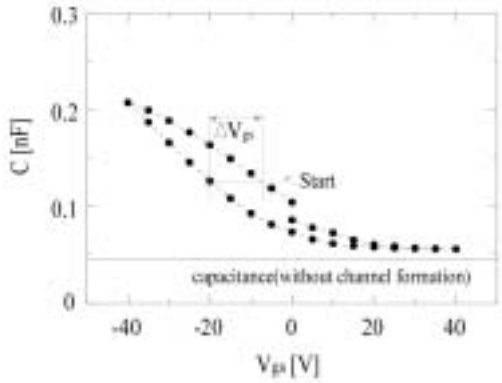

Fig. 1 The C-V measurement obtained for 100 nm pentacene FET using UV/ozone-OTS treated substrate

To further clarify the behavior of trapped carriers for V_{th} shift, we examined the hole trapping process by using the EFISHG that can probe the space charge formation in the FET channel [4]. For this purpose, we carefully examined the SHG at the off- and on-states of FETs by the repeated application of the different condition with V_g. Figures 2 (a) and (b) show the results of EFISHG and I_{ds} with respect to the elapsed scanning time, respectively. The applying bias sequence is as follows (see Fig 2); for Region (I) V_{ds}= 0 V, V_g= 0 V for 5 min, for Regions (II) and (IV) V_{ds}= -100 V, V_g= 0 V for 10 min (off-state) and for Regions (III) and (V) V_{ds}= -100 V, V_g= -100 V for 10 min and 20 min conditions (on-state), respectively. As shown in Fig. 2, SHG signal was very small in region I. On the other hand, in Region II the SH intensity enhances while the I_{ds} is nearly zero. This result indicates that the FET is off-states and SHG probes the Laplace field formed in the FET [4]. In region III, the SH intensity is small while the I_{ds} flows. This result indicates that the FET is on-states and SHG probes the poisson`s field formed in the FET. From these results, we may conclude that SH generation is depending on the Ids. SH intensity remarkably decayed with applying the gate voltage V_g,

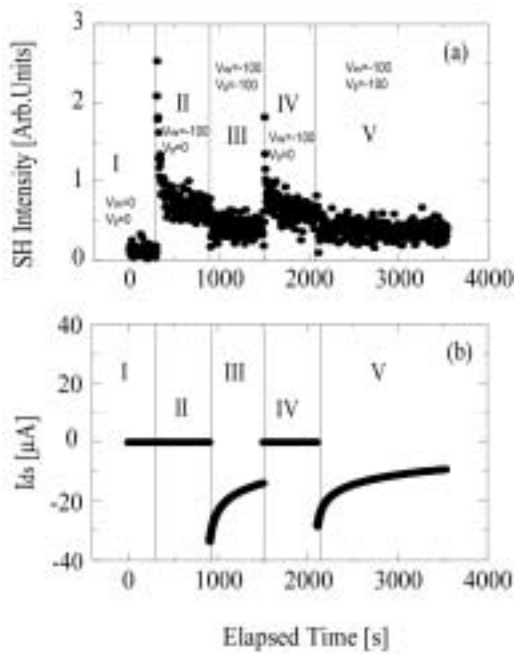

Fig. 2 Response of (a) the SHG with applying bias voltages and (b) the I_{ds} vs elapsed time for pentacene FET using UV/ozone-OTS treated substrate . Applied sequences are as follows; Region I (V_{ds}=0V, V_g=0V for 5 min.):Region II (V_{ds}=-100V, V_g=0V for 10 min.):Region III (V_{ds}=-100V, V_g=-100V for 10 min.):Region IV (V_{ds}=-100V, V_g=0V for 10 min.):Region V (V_{ds}=-100V, V_g=-100V for 20 min.)

indicating the channel formation, whereas the SH intensity enhanced in the absence of V_g indicating the destruction of the channel. Interestingly, the SHG and I_{ds} are generated similarly in region II and III, but the SHG generation in region II is somewhat stronger than that in region IV. This result indicates that during the I_{ds} flows in region III, some of the injected charge carriers are trapped at the interface between pentacene and SiO_2, and formed the space charge field. It should be noted that SHG decaying is seen in region II and IV. This is also related to the hole trapping, but the detail is under study. In the present study, we focused on the origin of the threshold voltage V_{th} shift observed in the FET characteristics.

References

[1] K. Ziemelis, Nature(London), **393** (1998) 619.

[2] C. D. Dimtrakopoulos, and D. J. Mascaro, IBM J. Res. & Dev. **45** (2001) 11.

[3] E. Lim, T. Manaka, R. Tamura, and M. Iwamoto, Jpn. J. Appl. Phys. **45**, (2006) 3712.

[4] T. Manaka, E. Lim, R. Tamura, and M. Iwamoto, Appl. Phys. Lett. **87**, (2005) 222107.