Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 924-925

D-8-5

Reduction of Bias-Induced Threshold Voltage Shift in Pentacene Field Effect Transistors by Interface Modification and Molecular Ordering

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1. Introduction

In recent years, organic field effect transistors (OFETs) have been receiving considerable interest due to their potentiality of application such as drivers for flexible displays, wireless identification tags, etc.[1] For these application, an important aspect of the organic FET is the stability both in ambient atmospheres and under TFT operation. However, the crucial instabilities are observed as a threshold voltage shift (ΔV_T) during bias stress and bi-directional gate sweep condition.[2] Also, the origin of threshold voltage shift has been debated although there are some candidates for explaining threshold voltage shift.[2]

The purpose of this work is to analyze synthetically the origin of the threshold voltage shift of OFETs and to propose an effective method for the reduction of ΔV_T under device operation.

2. Experimental Details

Transistors were fabricated in the top contact geometry. Heavily doped n^+-Si wafers were used both as a substrate and a gate electrode. Si wafers were thermally oxidized to be 50 nm thickness of SiO_2 to serve as a gate dielectric. Prior to active layer formation, the substrates were cleaned by 4:1 dilute H_2SO_4:H_2O_2 solution to remove organic contamination.

For the surface modification, samples were spilt with a formation of a 9.3 nm thick ploymethylmethacrylate (PMMA) layer and hexamethyldisilazane (HMDS) monolayer onto SiO_2 layers by spin-coating process. And these were baked at 100 °C during 30 minutes. In the final step, a 50 nm thick pentacene film was deposited using a thermal evaporation system, keeping the substrate temperature of 70 °C and deposition rate in the range of 0.4 Å/s. Afterward, Au was thermally evaporated on top of the pentacene layer using shadow masks giving transistors with various channel length and 800 μm width. The electrical characteristics of pentacene TFTs were measured in air and in the dark at room temperature.

3. Results and Discussion

Threshold voltages were measured as a function of gate voltage at a drain voltage of -5 V. Fig. 1(a) shows hysterisis of loop direction for the devices with W/L=800/80 μm based on SiO_2 dielectric without surface modification. After the gate bias sweeping between forward (+5 V → -10 V) and reverse (-10 V → +5 V), $|\Delta V_T|$ of 1.8 V was observed. In the set of Fig. 1(b) is also shown the capacitance-

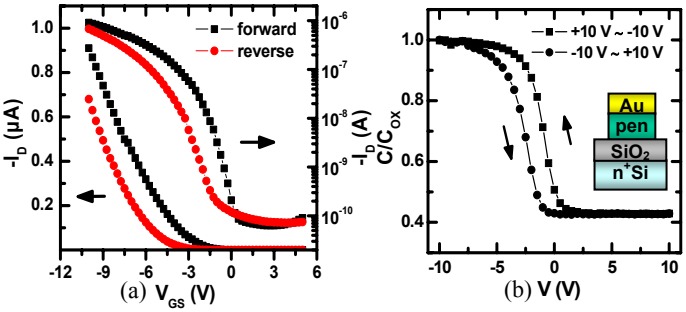

Fig. 1(a) Threshold voltage shit under bi-directional gate sweep: forward (+5 V→ -10 V) and reverse (-10 V → +5 V) (b) Hysterisis of loop direction for bi-directional voltage sweep.

voltage (C-V) characteristics for n^+-Si/SiO_2(50 nm)/pentacene(50 nm)/Au device. The flatband voltage shift of 2 V is accompanied by gate voltage sweep of -10 V → +10 V and +10 V → -10 V. A difference of threshold voltage under forward and reverse gate bias sweep could be generated by the charge trapping, mobile ions in the defect of insulator, interface or active layer itself. The carrier tunneling and mobile ions effect in insulator was dismissed in here since both cases have a low probability for the devices based on thermal grown oxide as a gate dielectric.

In order to verify the trapped carrier component, the gate voltage dependence of ΔV_T was measured after a fixed stressing time of 50 sec. During the gate bias stressing, source and drain were grounded. As illustrated in Fig. 2(a), ΔV_T of -3.8 V is shown to negative direction whereas ΔV_T of +0.3 V is followed into positive direction at -10 V and +10 V gate bias, respectively. The increased magnitude of ΔV_T further into negative direction indicates that ΔV_T is dominantly assigned by hole trapping. After stressing, an equal amount of charges per unit area is being accumulated

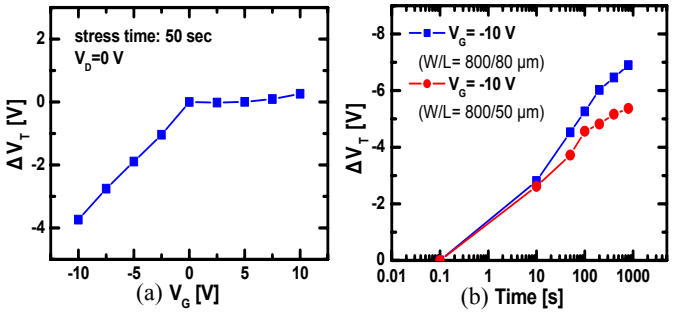

Fig. 2(a) Gate voltage dependence of threshold voltage shift under a fixed stressing time of 50 sec (b) Threshold voltage shift for transistors (W/L=800/80 μm and W/L=800/50 μm) as a function of time at a fixed gate bias of V_G=-10 V.

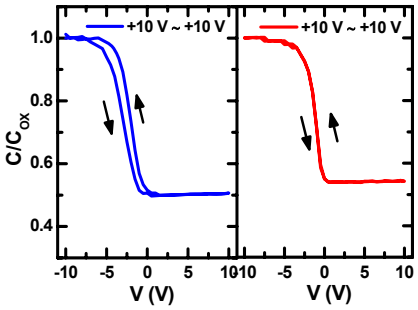

Fig. 3 Hysterisis of loop direction for HMDS- (left) PMMA (right) treated device.

up to ΔV_T in localized trap sites. Thus, if the trapping state is located uniformly in the interface between insulator and active layer, an increment of bias gives rise to larger threshold voltage shift by the leading of more deep level trapping.

But the trap site is still doubtful. Fig. 2(b) shows the time dependence of ΔV_T for the device of W/L=800/80 μm (squares) and W/L=800/50 μm (circles). The gate bias was fixed at V_G= -10 V as bias stress and source and drain were grounded. After 800 sec stress time, ΔV_T of -6.9 V and -5.3 V is inspected for the device with L_C=80 μm and L_C=50 μm, respectively. The result is shown the charge trapping is processed in slow trapping and also the trapping of charges is less mobile. More significantly, it is concluded that the charge trapping can be strongly affected by near the state of interface and accumulation regime in active layer since ΔV_T is continuously increased according to the stressing time. That is, as the carrier is injected from grounded electrodes into gate direction under gate bias stress, larger ΔV_T is generated when the charge is trapped near the state of interface and accumulation regime.

The surface properties are deeply depending on a molecular aggregation state of the surface.[3] The hydrophobic terminal state was provided by the surface modification with HMDS-[3] and PMMA[4] solutions on SiO_2 dielectric to reduce the mismatched interface terminal state between SiO_2 dielectric and pentacene active layer. After the surface modification with HMDS- and PMMA solution, The interface trap density (D_{it}) of $6.50\pm0.28\times10^{12}$, $3.20\pm 0.06\times10^{12}$ and $3.48\pm0.04\times10^{12}$ cm^{-2} ev^{-1} was estimated by using the subthershold current method [5] for non-treated, HMDS- and PMMA treated devices (W/L=800/80 μm), consecutively. The extracted D_{it} from the subthreshold swing (SS) variation of the TFTs is evidently shown the reduced interface trapping states by the surface modification on SiO_2.

Fig. 3 illustrates the reduced hysterisis behavior after each surface treatment. Flatband voltage shift of about 1 V is shown for HMDS treated device. While more interestingly, for PMMA treated case flatband voltage shift is lower than 0.01 V. Therefore, it is thought that a highly functionalized surface play a role to form more stable bonding state and reduce interface defect between interface and active layer.

The increase of electrical properties of organic device can be achieved by the film deposition at elevated tempatu-

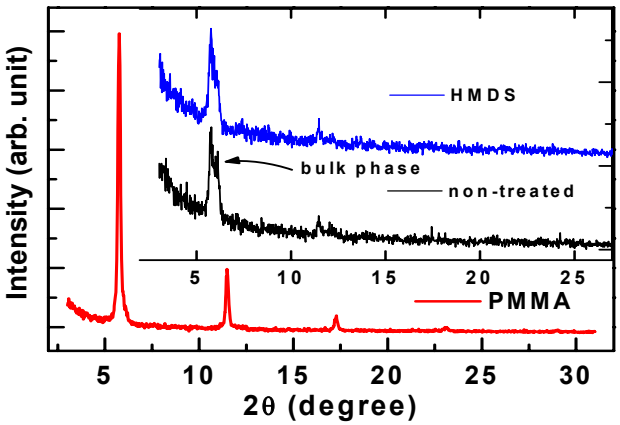

Fig. 4 XRD spectra of pentacene films with thickness of 50 nm at a substrate temperature of 70 °C for non-treated, HMDS and PMMA surface treated samples.

re which leads to large grain formation.[6] On the other hand, the reduced film crystallinity also is inspected from the film deposited at high temperature.[6] Therefore, in point of the stability of TFTs, the film deposition at elevated temperature can be brought device instability.

In Fig. 4 shows XRD result for 50 nm thick pentacene films deposited at 70 °C. The film on non-treated insulator shows the low crystalline characteristics including bulk phase. Whereas the increased crystallinity of thin film phase is shown for both HMDS- and PMMA treated samples. Especially, drastically well ordered thin film phase is achieved in the PMMA surface treated film even if the elevated substrate temperature. It denotes that the reduction of ΔV_T is also strongly affected by the efficient formation of the thin phase film since it may lead to the decrease of molecular trapping state in active layer. Conclusively, the threshold voltage shift caused by hole trapping is deeply correlated to molecular defect as well as interface state and also it can be reduced by the reduction of the interface trapping state and highly ordered film formation.

4. Conclusions

The origin of ΔV_T of OFETs was synthetically analyzed. Dominantly, ΔV_T is generated by hole trapping in the interface and active layer itself though more research is required for the quantitative comparison. An effective way was proposed to reduce of ΔV_T by the surface modification with PMMA surfactant on SiO_2 which diminishes the trapping site not only in the interface but in the active layer itself by providing hydrophobic terminal state in insulator and well ordered film formation even if the elevated substrate temperature.

References

[1] H. Klauk et al., IEEE Electron Device Lett. **20** (1999) 289.
[2] G. Gu et al., Appl. Phys. Lett. **87** (2005) 243512.
[3] S. C. Lim et al., Synth. Mat. **148** (2005) 75.
[4] X. Peng et al., Appl. Phys. Lett. **57** (1990) 2013.
[5] D. K. Schroder, Semiconductor Material and Device Characterization. (Wiley Interscience, 2006).
[6] J. Lee et al., Appl. Phys. Lett. **95** (2004) 3733.