Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 928-929

D-9-2

Low Hysteresis Organic Thin-Film Transistors and Inverters with Hybrid Gate Dielectric

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1. Introduction

Hysteresis characteristics of pentacene organic thin-film transistors (OTFTs) are very important for the electrical analysis and the operation of organic circuits. Hysteresis can introduce a significant error in analyzing electrical parameters such as field-effect mobility and threshold voltage. In addition, from the viewpoint of organic circuits, they are serious obstacles for reliable circuit operation. In this paper, in order to minimize hysteresis, pentacene OTFTs with hybrid gate dielectric are proposed and inverters with less hysteresis are implemented. Thickness optimization of the PECVD SiO_2/cross-linked PVA gate dielectric has demonstrated the effect of hysteresis reduction in OTFTs. The fabricated devices have several advantages including controllable low hysteresis characteristics and stable performance.

2. Device Fabrication

Fig. 1 shows the structure of the fabricated OTFT on oxidized silicon substrate. The titanium (Ti) gate electrode of 300 Å is evaporated and patterned by photolithography and wet etch. For the hybrid gate dielectric PECVD SiO_2 layer is deposited first, and as a second gate dielectric layer, 2 % PVA solution mixed with ammonium dichromate photo-sensitizer is spin-coated and cross-linked by UV exposure [1]. The hybrid gate dielectric is patterned by photolithography and dry etch. The gold (Au) source/drain electrodes are patterned by photolithography and lift-off process. The device is completed using thermal evaporation of pentacene at high vacuum ambient of around 10^{-8} Torr. The substrate temperature is 80 ℃, and the active region is patterned by a shadow mask.

3. Results and Discussion

Fig. 2 shows the hysteresis in the transfer characteristics of cross-linked PVA monolayer gate dielectric OTFT. The charges injected to the PVA bulk or interfaces bring about a large threshold voltage (V_T) shift [2]. This V_T shift might cause a malfunction of organic circuits. On the other hand, Fig. 3 illustrates the reduced hysteresis of OTFTs using PECVD SiO_2/cross-linked PVA gate dielectric. Here, the sweep voltage ranges are determined differently to compare the devices at the same electric-field, considering the thickness and dielectric constant of gate dielectric layers. The obvious trend of hysteresis as a function of the thickness of SiO_2 is observed in the figure. Fig. 3(a) shows opposite hysteresis behavior to 3(c) and 3(d), according to the sweep direction. This trend indicates the existence of optimum thickness for the hybrid gate dielectric. Among the four devices, the least hysteresis is found in the device with 3(b) condition which has PECVD SiO_2 of 350 Å and cross-linked PVA of 950 Å gate dielectric.

Fig. 4 shows the concept of hysteresis reduction mechanism. When the negative gate bias is applied, the SiO_2 layer blocks the charge (electron) injection from the gate electrode, hence the V_T shift is reduced. However, when the SiO_2 layer is thick enough to block most electrons, the effect of hole trap from the pentacene appears. According to this mechanism, an optimum condition exists for the least hysteresis. Fig. 5 illustrates the transfer characteristics of optimized OTFTs with various channel lengths, verifying the hysteresis reduction effect of the hybrid gate dielectric. Device parameters for W/L=300/5, under saturation conditions, are as follows: field-effect mobility, $\mu = 0.12$ cm^2/V·sec, subthreshold slope, SS = 0.4 V/dec, and on/off ratio = 1.3×10^8. The performances are attributed to the high dielectric constant and the low off-current of PECVD SiO_2/cross-linked PVA gate dielectric.

To investigate the circuit operation, an inverter consisting of an enhancement mode driver and a load is implemented. The schematic diagram of the integrated inverter and the voltage transfer curves are shown in Fig. 6. The inverter with PECVD SiO_2/cross-linked PVA gate dielectric shows considerably reduced hysteresis compared to the inverter with cross-linked PVA monolayer gate dielectric.

4. Conclusions

Easily controllable low hysteresis pentacene OTFTs are fabricated with PECVD SiO_2/cross-linked PVA gate dielectric. The hysteresis reduction is achieved by thickness optimization of the hybrid gate dielectric. The proposed hybrid gate dielectric insures reliable operations of the OTFTs and organic circuits.

Acknowledgements

This work was supported by "Samsung SDI – Seoul National University Display Innovation Program".

References

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[2] Th. B. Singh et al., *Appl. Phys. Lett.,* **85** (2004) 5409.

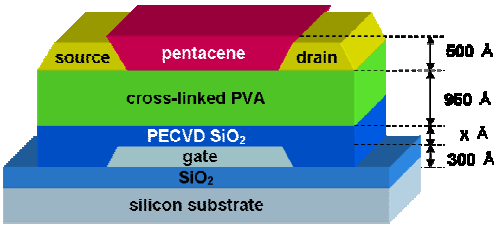

Fig. 1. Structure of bottom-contact pentacene OTFT with PECVD SiO_2/cross-linked PVA hybrid gate dielectric.

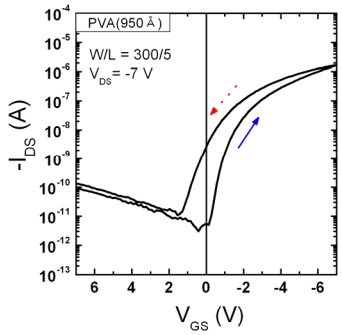

Fig. 2. Hysteresis characteristics of cross-linked PVA monolayer gate dielectric OTFT. A large V_T shift according to the sweep direction is observed.

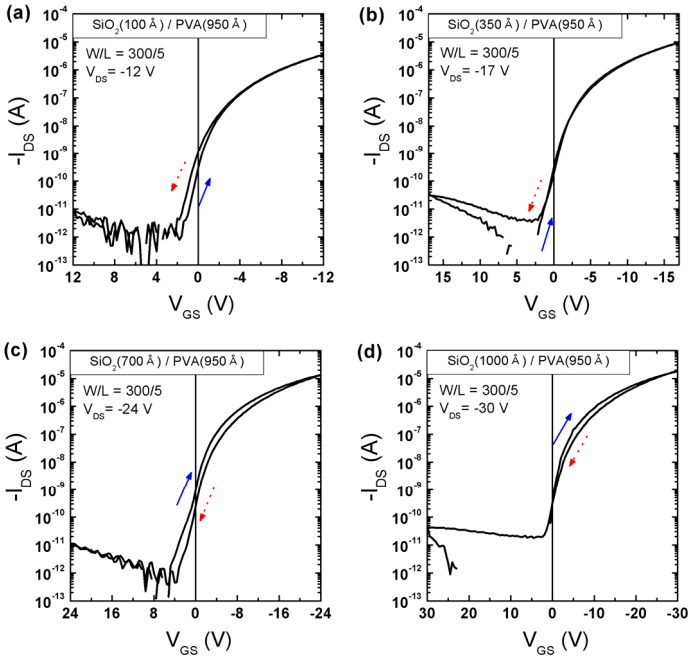

Fig. 3. Hysteresis characteristics of PECVD SiO_2/cross-linked PVA gate dielectric OTFTs. The thickness of PECVD SiO_2 are (a)100 Å, (b)350 Å, (c)700 Å, and (d)1000 Å. The least hysteresis is shown in 3(b).

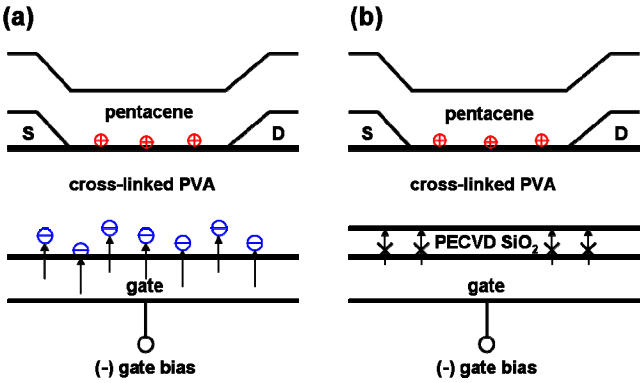

Fig. 4. Concept of hysteresis reduction mechanism (a) Charge injection from the gate electrode cause the V_T shift. (b) PECVD SiO_2 layer blocks the charge injection so that the hysteresis is reduced.

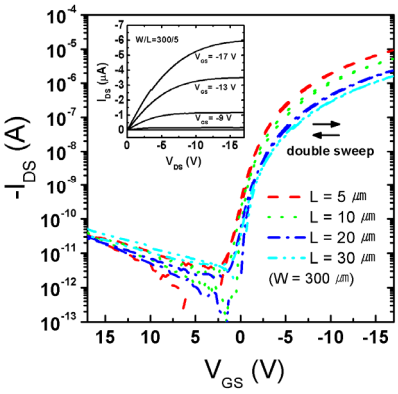

Fig. 5. Hysteresis characteristics of optimized OTFTs for various channel length. Inset: output characteristics of OTFT with L=5 ㎛.

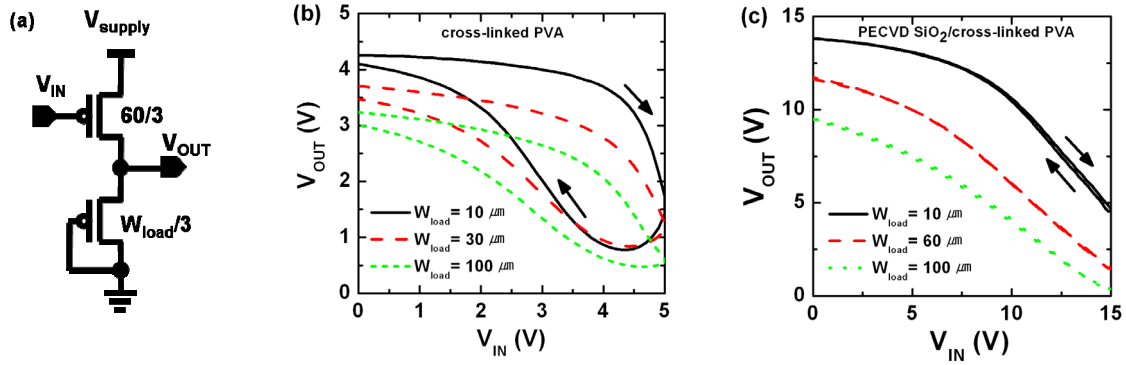

Fig. 6. (a) Schematic diagram of the inverter (b) Voltage transfer curves (VTC) for cross-linked PVA monolayer gate dielectric (c) VTC for PECVD SiO_2/cross-linked PVA gate dielectric. The inverter with PECVD SiO_2/cross-linked PVA gate dielectric shows considerably reduced hysteresis.