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InP-based High-speed Transistors and Their IC Applications

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1. Introduction

The research and development of InP-based devices and ICs are driven by applications in broadband optical-fiber communications systems and microwave and millimeter-wave wireless systems. This paper describes recent progress on our InP-based high-speed transistors and IC technologies, especially for 40-Gbit/s optical fiber communications and 120-GHz band millimeter-wave wireless links for 10-Gbit/s data transmission. Device performance requirements for future 100-Gbit/s class data transmission ICs are then discussed along with our latest IC results.

2. 40-Gbit/s Optical Communication ICs

In optical fiber communications, 10-Gbit/s systems now have a large commercial market, and work on the technological aspects of 40-Gbit/s ICs has reached the stage where cost-effective commercial products are being developed [1]. Enlarging the tolerance to dispersion is an important issue for high-bit-rate long-haul transmission, because chromatic dispersion and polarization mode dispersion are major factors limiting the transmission distance. Electrical dispersion compensation techniques are expected to reduce the size, power and cost of the systems, compared with the reductions possible with conventional optical dispersion compensation.

We have designed two 40-Gbit/s equalizer ICs: a linear equalizer as a feed-forward equalizer (FFE) and a nonlinear equalizer as a decision feedback equalizer (DFE), both fabricated using 1.0- μm -emitter-wide InP HBTs [2]. Figure 1 shows a receiver configuration, in which the FFE and DFE as well as an eye-opening monitor and a controller are arranged following the linear baseband amplifiers. These ICs were tested separately. Figure 2 shows an operating waveform of the FFE IC at 40 Gbit/s. Both ICs were confirmed to be able to compensate differential group delay of over 20 psec for 40-Gbit/s NRZ signal.

3. ICs for 120GHz-band Wireless Links

The bit-rate increases in the data communications are also creating new demands for high-speed wireless local area networks and personal area networks. Recently, 10-Gbit/s wireless links are expected to be used as temporary broadband networks in natural-disaster recovery efforts, at event halls, and for remote broadcasts [3].

The upper half of the F band is suitable for 10-Gbit/s data transmission because of sufficient bandwidth, ease of hardware implementation, and moderate attenuation due to oxygen absorption. The carrier frequency of the system is 123 GHz, and the modulation scheme is currently amplitude shift keying (ASK). The transmitter (Tx) consists of a frequency doubler, an ASK modulator with a traveling-wave switch, an RF band-pass filter, and power amplifiers, while the receiver (Rx) consists of low-noise amplifiers and an ASK demodulator. We designed and fabricated the Tx and Rx using 0.1- μm -gate-length InP HEMTs [4]. All the components needed for the Tx and Rx were monolithically integrated on a single chip.

The measured back-to-back performance and the received 10-Gbit/s data signal at -38.7 dBm input are shown in Fig. 3. The Rx sensitivity of -45.7 dBm was obtained. The estimated possible transmission distance is 200 m for the 10-Gbit/s data rate, assuming the use of a lens antenna with gain of 45 dBi and a rain intensity of 25 mm/hr (attenuation: 12-dB/km).

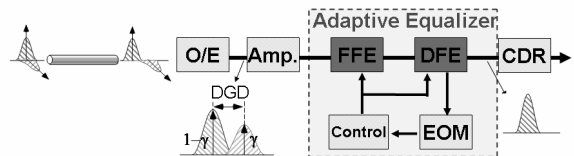


Fig. 1. Receiver configuration with equalizer ICs.

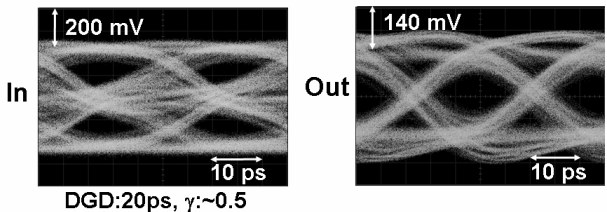


Fig. 2. Operating waveforms of the FFE IC at 40 Gbit/s.

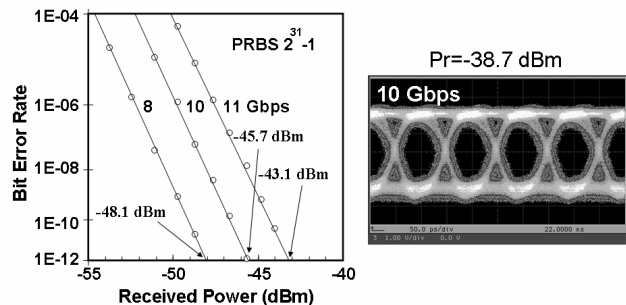


Fig. 3. Back-to-back test results and received eye-pattern.

4. Device and ICs for Future 100-Gbit/s Class Data Transmissions

Device Performance

Table 1 shows our InP HBT technology roadmap. The epitaxial layers are grown by MOCVD for all generations. The emitter is scaled down from a width of 2 μm for the first generation to 0.8 μm for the third generation (G3). The base and collector layers for the G3-DHBT have been thinned to 30 and 150 nm, respectively. The measured typical f_T and f_{max} of the 150-nm-thick-collector G3-DHBT are around 320 GHz at collector current density of 5 $\text{mA}/\mu\text{m}^2$ [5]. The measured minimum emitter-coupled logic (ECL) gate delay time of the HBT is 3.48 ps. A G3-DHBT with a 0.6- μm -wide emitter exhibits an f_T of around 340 GHz and an f_{max} of 492 GHz at collector current density of 6 $\text{mA}/\mu\text{m}^2$.

Calculated ECL gate delay contours along with the performance of state-of-the-art devices are shown in Fig. 4. As shown in this figure, the G3-DHBT has the potential to achieve 100-Gbit/s static D-type Flip-Flop (DFF) operation. In addition, some further-scaled-down HBTs with an emitter width of less than 0.6 μm exhibit an f_T of around 400 GHz and an f_{max} of around 500 GHz, which are close to the requirements for 160-Gbit/s DFF operation.

IC Results

We have designed and fabricated a TIA [6] and a 2-bit MUX [7] using the G3-DHBTs. The TIA consists of a parallel-feedback amplifier core and a cascade-type output buffer. Measured gain and 3-dB bandwidth are 14 dB and 91 GHz, respectively. We also confirmed clear eye opening in the output eye diagram at 100 Gbit/s.

Table 1 Roadmap for NTT's InP HBT

Parameter	1st Generation	2nd Generation	3rd Generation
Epitaxial Growth	MOCVD	MOCVD	MOCVD
Base Doping	Zn	C	C
Emitter Width	2 μm	1.0 μm	0.8 μm
Base Thickness	50 nm	50 nm	30 nm
Doping	$4 \times 10^{19} \text{ cm}^{-3}$	$4 \times 10^{19} \text{ cm}^{-3}$	$6.0 \times 10^{19} \text{ cm}^{-3}$
Sheet Resistance	600 Ω/\square	600 Ω/\square	600 Ω/\square
Collector Thickness	300 nm	300 nm	150 nm
Current Density	0.5 $\text{mA}/\mu\text{m}^2$	1.0 $\text{mA}/\mu\text{m}^2$	5.0 $\text{mA}/\mu\text{m}^2$
f_T	$\sim 100 \text{ GHz}$	$\sim 150 \text{ GHz}$	$> 300 \text{ GHz}$
f_{max}	$\sim 150 \text{ GHz}$	$\sim 250 \text{ GHz}$	$> 300 \text{ GHz}$

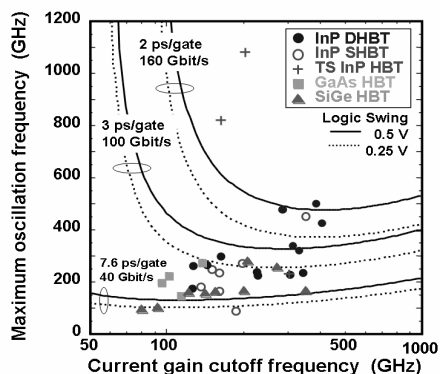


Fig. 4. Gate delay time contours for ECL inverters.

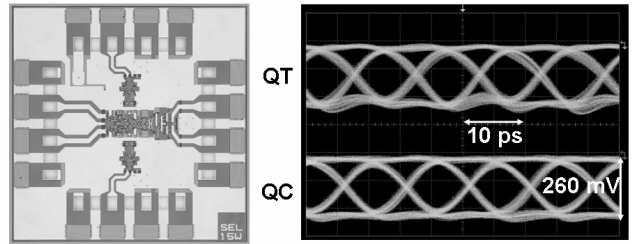


Fig. 5. Chip photograph and operating waveform of the MUX IC.

The MUX is based on a two-stage series-gated ECL. It is important to design the operating condition so that the HBTs have not only a high f_T and f_{max} but also a high collector current density for high-speed circuit operation. The current density of the HBTs is set to a relatively high of 5 $\text{mA}/\mu\text{m}^2$. Figure 5 shows a chip photograph and the operating output waveforms at 100 Gbit/s, respectively. Clear eye opening is obtained with an output voltage of 260 mV and an RMS jitter of 400fs.

5. Conclusions

We described InP-based device and IC technologies for optical fiber communications and for a 10-Gbit/s data transmission wireless link. The research interest in 40-Gbit/s optical communications ICs has shifted from basic ICs to highly integrated and functional ones, such as those for electrical dispersion compensation. Research on devices and ICs for future 100-Gbit/s-class systems is underway, and some basic ICs have been successfully demonstrated at over 100 Gbit/s. State-of-the-art InP HBTs with a half-micrometer-wide emitter have potential for 160-Gbit/s-class ICs.

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References

- [1] K. Murata, K. Sano, H. Fukuyama, Y. Yamane, Y. K. Fukai, H. Kitabayashi, H. Sugahara, and T. Enoki, IEEE GaAs IC Symposium Proceeding (2003) 161.
- [2] M. Nakamura, H. Nosaka, M. Ida, K. Kurishima, and M. Tokumitsu, Optical Fiber Communication Conference Proceeding (2004) TuG4.
- [3] T. Nagatsuma and A. Hirata, NTT Technical Review 12 (2004) 58.
- [4] T. Kosugi, M. Tokumitsu, T. Enoki, M. Muraguchi, A. Hirata, and T. Nagatsuma, IEEE Compound Semiconductor IC Symposium Proceeding (2004) 171.
- [5] M. Ida, K. Kurishima, K. Ishii, and N. Watanabe, 2003 IEEE GaAs IC Symposium Proceeding (2003) 211.
- [6] H. Fukuyama, K. Sano, M. Ida, K. Kurishima, K. Murata, K. Ishii, T. Enoki, and H. Sugahara, 16th Indium Phosphide and Related Materials Conference Proceeding (2004) 659.
- [7] K. Sano, K. Ishii, K. Murata, K. Kurishima, M. Ida, T. Shibata, T. Enoki, and H. Sugahara, International Conference on Solid State Devices and Materials Proceeding (2004) 312.