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High-speed and Low-Power NRZ Delayed Flip-Flop Circuit Using RTD/HEMT Integration Technology

Hyungtae Kim, Seongjin Yeon, and Kwangseok Seo

Seoul National Univ., School Of Electrical Engineering and Computer Science
San 56-1, Shillim-dong, Kwanak-ku, Seoul 151-744, Korea
Phone: +82-2-877-0298 E-mail: kimhemt@hanmail.net

1. Introduction

After MOnostable-to-BIstable transition Logic Element (MOBILE) was proposed [1], the monolithic integration of RTD and conventional transistors has attracted much attention for high-speed digital circuit application. However, MOBILE-based circuits are not compatible to conventional logic circuits because MOBILE-based logic circuits' outputs are return-to-zero (RZ) mode. To overcome this problem, MOBILE-based delayed flip-flop (D-F/F) circuits with non-return-to-zero (NRZ) mode output were implemented by combining original MOBILE with set/reset flip-flop [2]-[4]. Even though these circuits have the advantage of reduced device count over the conventional MS D-F/Fs, they use about twice the devices and the power consumption of the circuit increases compared to original MOBILE.

In this paper, we propose a new NRZ-mode D-F/F circuit using RTD/HEMT integration technology on an InP substrate. The operation of the fabricated D-F/F is demonstrated up to 26 Gb/s with low power consumption of about 3 mW.

2. Circuit configuration and operation principle

Figure 1 shows the circuit configuration of proposed D-F/F with NRZ-mode output. The key point of the proposed circuit is that it uses the switching sequence control of two serially connected RTDs and the switching is driven by oscillating the clock voltage. The output state is determined by the switching characteristics and self latching characteristics of RTDs, which is explained later in this section. The proposed D-F/F core is composed of RTD/HEMT parallel connection (Q1, RTD1) and RTD/HEMT series connection (Q2, RTD2) which is used in the data input stage and in the clock input stage, respectively. Moreover, in order to minimize measurement system effect buffers for data, clock, and output are included in the circuit.

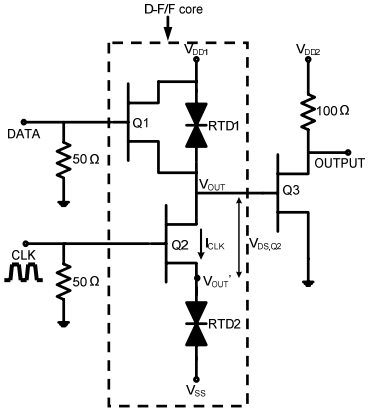
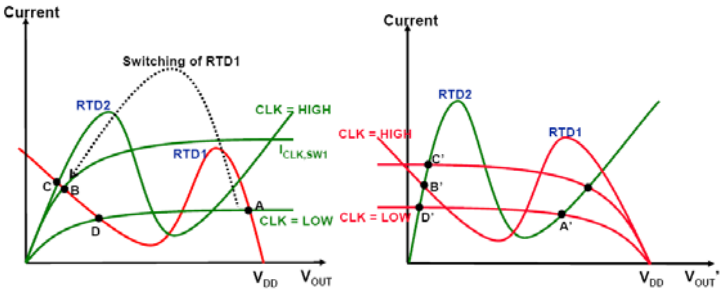
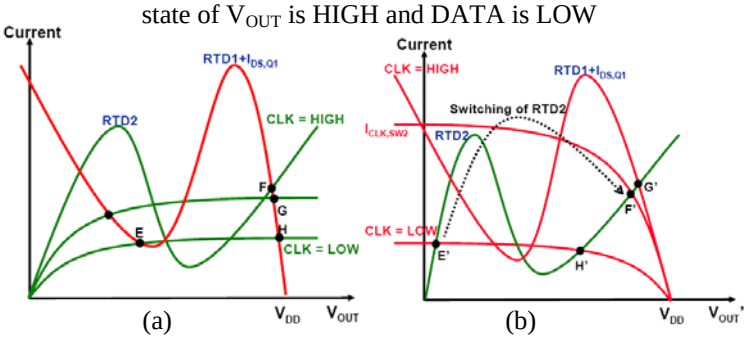


Fig. 1 Circuit configuration of proposed NRZ D-F/F



(a) (b)

Fig. 2 Load line diagram of NRZ D-FF when initial state of V_{OUT} is HIGH and DATA is LOW



(a) (b)

Fig. 3 Load line diagram of NRZ D-FF when initial state of V_{OUT} is LOW and DATA is HIGH

This new circuit configuration has two advantages over the previously reported MOBILE-based D-F/Fs. First, NRZ-mode output is generated using drastically reduced circuit complexity with low power consumption. Second, clock loading is decreased because clock is isolated from the circuit by feeding clock into the gate of HEMT (Q2).

The operation of the proposed D-F/F is similar to that of the original MOBILE circuit when clock is HIGH [1], [5]-[7], but different when clock is LOW because RTD/HEMT series connection has the RTD-like I-V characteristics when drain current of HEMT(Q2) is larger than RTD's peak current(RTD2) and FET I-V characteristics when drain current of HEMT is smaller than RTD's peak current. For proper operation, the area of the upper RTD (RTD1) is designed to be smaller than that of the lower RTD (RTD2). The data value is designed so that the current through Q1 is smaller than the peak current difference of RTD1 and RTD2 when data is LOW, and lager than the peak current difference when data is HIGH. The clock HIGH value is chosen to make drain current of Q2 larger than the peak current of parallel connection of RTD1 and Q1 when DATA is HIGH and the clock LOW value is designed to be larger than threshold voltage of Q2 to make the circuit bistable when clock is LOW as shown in Fig. 2 and

Fig. 3.

Figure 2(a) shows the load line diagram of the proposed D-F/F with respect to V_{OUT} when initial state of V_{OUT} is HIGH and DATA is LOW. Figure 2(b) shows the load line diagram with respect to V_{OUT}'. V_{OUT} and V_{OUT}' have the same logic property with a voltage offset of $V_{DS,Q2}$. Thus the initial state of V_{OUT}' is also HIGH. When I_{CLK} is larger than $I_{CLK,SW1}$ as the clock increases, the RTD1 switches to 2nd positive differential resistance region(PDR) (A to B and A' to B' in Fig. 2.). Thus V_{OUT} and V_{OUT}' latch to LOW. (State C for V_{OUT} and state C' for V_{OUT}' is the final state after LOW to HIGH transition of clock.) As clock decreases to LOW, the state moves to the closest stable state by the self latching characteristic of RTD (C to B and B to D for V_{OUT}, C' to B' and B' to D' for V_{OUT}' in Fig 2). Thus V_{OUT} latches HIGH to LOW at the rising edge of the clock and remains at LOW when clock decreases to LOW. If DATA maintains its value at LOW after the switching process, RTD1 remains at 2nd PDR and RTD2 remains at 1st PDR because no switching process takes place during clock transition. Thus V_{OUT} and V_{OUT}' remain at LOW.

Now it is assumed that DATA changes LOW to HIGH. Figure 3(a) shows the load line diagram of the proposed D-F/F with respect to V_{OUT} and Fig. 3(b) shows the load line diagram with respect to V_{OUT}'. When I_{CLK} is larger than $I_{CLK,SW2}$ as the clock increases, the RTD2 switches to 2nd PDR as shown in Fig. 3(b). As clock decreases to LOW, the state moves to the closest stable state. Thus V_{OUT}' and V_{OUT} switches LOW to HIGH at the rising edge of the clock and remains at logic HIGH when clock decreases to LOW. The states are described by (E, F, G, H) for V_{OUT} and (E', F', G', H') for V_{OUT}' in Fig. 3.

Consequently, the proposed D-F/F core circuit generates a non-inverted NRZ-mode output according to DATA. The overall circuit functions as an inverted D-F/F with NRZ-mode output because the output buffer is simple DCFL inverter.

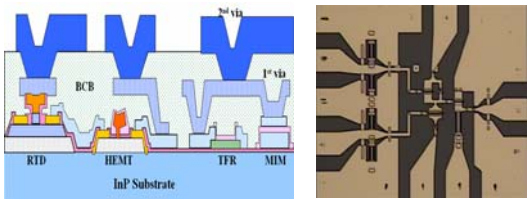
3. Device structure and fabrication

We integrated AlAs/InGaAs/InAs RTD and InAlAs/InGaAs HEMT monolithically on an InP substrate. The epitaxial layers were grown by MBE and the devices were fabricated using optical lithography, e-beam lithography and lift-off process. Figure 4(a) shows the cross-sectional view of the fabricated ICs and Fig. 4(b) shows the microphotograph of the fabricated D-F/F.

The peak current density of the fabricated RTDs was 112 kA/cm^2 with a good peak-to-valley current ratio of 12. The peak voltage of the fabricated RTD was 0.3 V. Fabricated 0.1 um HEMT showed the maximum transconductance of 1.2 S/mm with the threshold voltage of -0.55 V. The maximum cutoff frequency was about 220 GHz.

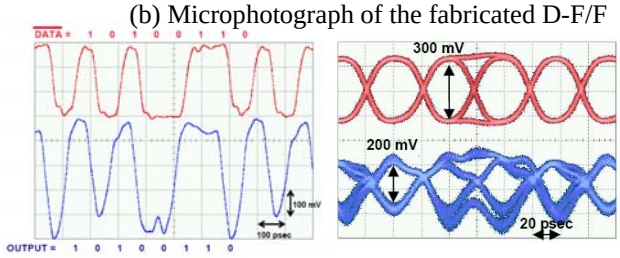
4. Measurement result

Figure 5(a) shows the result at 12.5 Gb/s with an input bit pattern of (01011001). The upper trace is the complement of the input data stream. The lower trace shows the output waveform. The output is complement of the input because the output buffer is DCFL inverter. The output amplitude was about 500 mV.



(a) (b)

Fig. 4 (a) Cross sectional view of the fabricated IC
(b) Microphotograph of the fabricated D-F/F



(a) (b)

Fig. 5 Measurement result of the fabricated NRZ D-F/F

Figure 5(b) shows the results of operation with the input of a quasi-pseudo-random bit stream at 26 Gb/s. Upper trace shows the DATA eye patterns and lower trace shows the output eye patterns. Clear NRZ mode eye patterns with about 200 mV eye opening were obtained at this bit rate as shown in Fig. 5 (b). These results confirm the proper operation of the fabricated D-F/F up to 26 Gb/s.

5. Conclusion

A new NRZ D-F/F circuit with drastically reduced circuit complexity is proposed and fabricated using RTD/HEMT integration technology on an InP Substrate. The proposed circuit uses only 4 devices (2 RTDs and 2 HEMTs), by utilizing switching and self latching properties of RTDs, which is the minimum device count to implement NRZ D-F/F up to now. The operation of the fabricated circuit is confirmed up to 26 Gb/s. And the power consumption of the fabricated D-F/F core circuit is about 3 mW. This result indicates the great potential of the proposed circuit for high-speed and low-power digital IC applications.

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