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Thermally-stable gate technologies for InAlAs/InGaAs/InP HEMTs

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1. Introduction

Due to its superior high frequency and low-noise capabilities, InAlAs/InGaAs/InP high electron mobility transistors (HEMTs) are the most promising devices for high speed digital circuit and sub-millimeter-wave applications. Among the various problems limiting their applications, the thermal stability of the gate contacts is still a big reliability concern. Thermal reliability studies show that gate-sinking is the major degradation mechanism and it causes non-reversible device failure.[1] Compared with the depletion mode HEMTs (D-HEMTs) technology, the requirement of gate technology for enhancement-mode HEMTs (E-HEMTs) is more stringent. For E-HEMTs, a high Schottky barrier height (φ_B) of over 800 meV is usually needed. Meanwhile, in order to deplete the channel layer at zero applied voltage, a short gate-to-channel distance is required. For this reason, in-diffusion of gate metal could easily modify key device operation parameters, such as transconductance, threshold voltage, and gate capacitance, or even cause device failure during prolonged thermal/electrical stress. Pt-based gate used for E-HEMTs has a high Schottky barrier height on InAlAs,[2] but Pt diffuses rapidly in InAlAs at temperatures as low as 250 °C.[3]

In this paper, we report on Ir-based gate technologies developed in our group.[4,5] We show that Ir gate on InAlAs has a high Schottky barrier height of over 800 meV after being annealed at over 400 °C. Thermal storage test at 215 °C shows no electrical performance degradation and structural alteration. Devices fabricated using Ir gate showed excellent DC and RF performance as well as superior thermal stability. Cross-sectional transmission electron microscopy (TEM) studies were carried out to correlate the electrical performance with the structural evolution.

2. Experimental

In order to measure φ_B of Ir gate as a function of annealing temperature, Schottky diodes using Ir/Ti/Pt/Au contacts with a diameter of 250 μm were deposited on MBE-grown InAlAs/InP heterostructures. The heterostructure contains a 0.1 μm-thick n^+ InAlAs buffer layer followed by a lightly doped 0.9 μm-thick- InAlAs all grown on n^+-InP. On the InP backside, AuGe/Ni/Au blanket ohmic contact was deposited and annealed. The Schottky metallizations were then deposited on InAlAs. The diodes were annealed at different temperatures for 30 s under N_2 ambient in a RTA system. φ_B was subsequently measured. For TEM studies, Schottky metals were deposited directly on HEMTs wafers,[5] after the InGaAs cap layer, D-HEMTs barrier layer and AlAs etch stop were removed. TEM samples were prepared by sample gluing, grinding and ion milling on a liquid N_2 cooling stage. Scanning TEM (STEM) was used to form Z-contrast images on a JEOL 2010F TEM operated at 200 kV. Energy dispersive X-ray spectroscopy (EDS) signals were collected and were used to quantify local composition.

3. Results and Discussions

Figure 1 shows the measured φ_B as a function of annealing temperature for several metallization schemes. It is evident from this plot that the optimum φ_B are achieved at ~ 425 °C for all schemes. As the Ir layer thickness increases, optimum φ_B also increases and the best φ_B of 820 meV is obtained for the scheme with 10 nm Ir. Slow and monotonic enhancement of φ_B below 425 °C is observed, while for the schemes with 2.5 and 5 nm Ir, φ_B decreased to below 500 meV with further increase in temperature. 5 nm-Ir scheme shows a somewhat slow decreasing rate. In contrast, the 10 nm-Ir scheme demonstrated a different behavior with φ_B degrading rather slowly and φ_B remaining over 780 meV even when annealed at 500 °C. Similar φ_B enhancement mechanism exists for all schemes; however, different degradation mechanisms of φ_B seem to exist. The optimum annealing temperature of the Ir gate is much higher than that for Pt gate, which means that Ir gate is intrinsically much stable than Pt. Wider temperature latitude also exists for Ir gate. Samples with 10 nm Ir stored at 215 °C for over 200 h shows no sign of performance degradation.

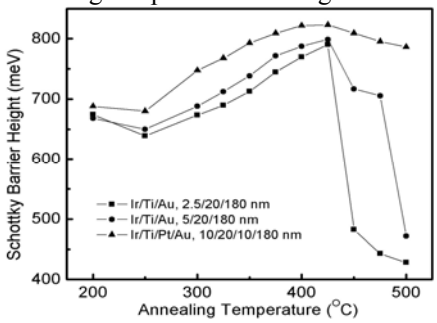

Fig. 1 φ_B vs. annealing temperature.

To examine the relationship between the Schottky barrier characteristics and Ir/InAlAs interfacial reactions at different annealing temperatures, and more importantly to scrutinize the enhancement and degradation mechanism of the contact schemes, cross-section TEM studies were carried out on blanket-deposited samples that were annealed at different temperatures: as-deposited, annealed at 325 °C, 425 °C and 475 °C. Two contact schemes, namely, Ir/Ti/Pt/Au (2.5/20/10/160 nm) and (10/20/10/160 nm), were investigated and compared.

Figure 2 is an HRTEM micrograph of the interfacial area for the 10 nm-Ir gate before annealing. It is seen that the Ir lattice does not readily transfer to that of InAlAs, and an amorphous layer (a-layer) of 0.6 nm thick is observed at the interface. Similar result was obtained for the 2.5 nm-Ir contact. Annealing causes the thickening of this a-layer due

to intermixing of Ir with InAlAs. For the 10 nm-Ir sample, this a-layer thickness increases to ~ 2.5 nm (see Fig. 3) and it has an average composition of 4 % Al (at. %, 36 % As, 31 % In and 29 % Ir as measured by EDS.

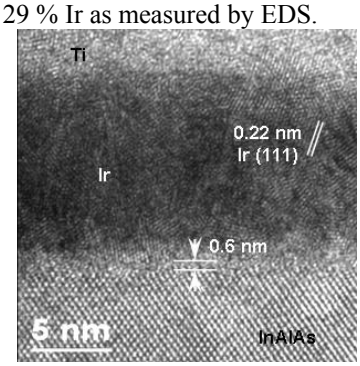

Fig. 2 HRTEM image of as-deposited 10 nm-Ir contact.

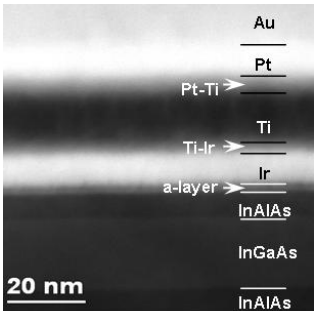

Fig. 3 STEM image of 425 °C annealed 10 nm-Ir contact.

At over 425 °C, φ_B starts to degrade and concurrently we observed the crystallization of the a-layer, as indicated in Fig. 4. Measured from the interplanar distance and composition of the crystals, this crystalline phase is identified to be monoclinic $IrAs_2$.

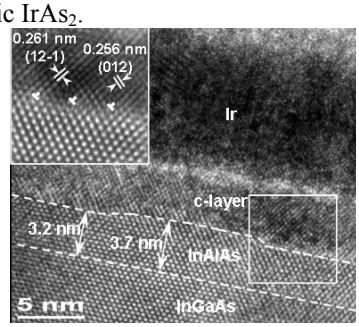

Fig. 4 HRTEM image of 475 °C annealed 10 nm-Ir contact.

For the 2.5 nm-Ir gate, completely different reaction pathway is observed. Figure 5 shows the HRTEM image of the interface after 475 °C annealing and EDS line scans for the metals across the interfacial area. Unlike the 10 nm-Ir case, the a-layer with a thickness of 1.7 nm remains even after this high temperature annealing. EDS analyses show that this a-layer has high content of Ti suggesting that 2.5 nm thick Ir is not enough to block the in-diffusion of Ti. Infact, in the Ir layer, a high Ti content of 36 % is detected. The EDS line scans of Fig. 5(b) indicates that the Ir layer is completely engulfed by the Ti layer so that a mixture of Ir and Ti is in direct contact with the InAlAs. Since Ti has a low φ_B of 500-600 meV, the acute overannealing degradation of 2.5 nm-Ir gate in Fig. 1 is due to Ti in-diffusion. On the other hand, the thicker Ir (e.g. 10 nm) is sufficient to prevent the in-diffusion of Ti so that φ_B of the 10 nm-Ir follows a different deterioration mechanism. Detailed investigations of Fig. 4 suggest that the transformation of a-layer to c-layer accounts for the change in φ_B of the 10 nm-Ir sample. We conjecture that the $IrAs_2$ phase has a lower φ_B than that of the amorphous mixture of Ir with InAlAs.

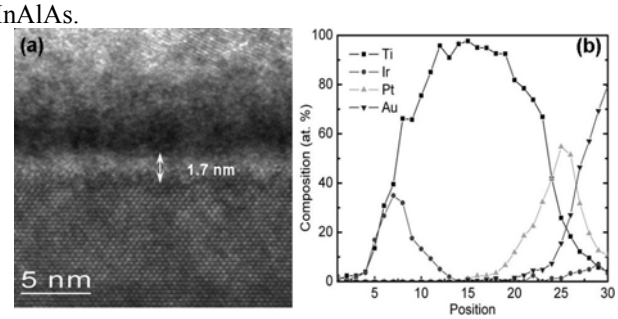

Fig. 5 (a) HRTEM image of 475 °C annealed 2.5 nm-Ir contact; (b) EDS composition scan across the interfacial area.

4. Conclusion

The Schottky barrier heights of Ir gate metallizations for InP-HEMTs were studied as function of annealing temperature. It is observed that φ_B depends on both Ir thickness and annealing temperature. Optimum φ_B of 820 meV is obtained for the 10 nm-Ir sample annealed at 425 °C. φ_B of Ir is higher than that of Pt gate and the high annealing temperature of Ir suggests that it has higher thermal stability than Pt. TEM studies show that the a-layer formation is responsible for φ_B enhancement. Ti in-diffusion results from overannealing for schemes with thin Ir layer. The crystallization of the a-layer into $IrAs_2$ is responsible for the degradation of the thick Ir scheme. This thick Ir-gate technique should be effective for reliable InAlAs/InGaAs/InP HEMTs

Acknowledgements

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