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The Gate Length Reducing Process for Pseudomorphic $In_{0.52}Al_{0.48}As/In_{0.7}Ga_{0.3}As$ HEMTs

Seong-Jin Yeon, Jongwon Lee, Gyungseon Seol, Kwangseok Seo

Seoul National Univ., School Of Electrical Engineering and Computer Science
San 56-1, Shillim-dong, Kwanak-ku, Seoul 151-744, Korea
Phone: +82-2-877-0298 E-mail: realzeratol@hanmail.net

1. Introduction

InP-based InAlAs/InGaAs high-electron mobility transistors have a good DC and RF characteristics, owing to their higher electron mobilities, saturation velocities, and sheet electron densities [1]. Many groups reported superior RF characteristics of HEMTs by reducing gate length [2]-[3]. But, reducing gate length needs high resolution E-Beam lithography system. Also narrow gate pattern smaller than 50nm has gate metal filling issue due to high aspect ratio. To solve this problem, we developed gate length reducing process. Through this process, initial gate length of 130nm was reduced to sub-30nm. This process enables to achieve narrow pattern beyond limit of E-Beam lithography and also solve metal filling problem.

2. Epitaxial Structure and Process

The epitaxial structure of the studied devices was $In_{0.7}GaAs/In_{0.52}AlAs$ Pseudomorphic HEMT grown by molecular beam epitaxy (MBE) on a InP substrate, yielding a mobility of 10,800 cm^2/V-s and a sheet carrier density of $3.31x10^{12}/cm^2$ at 300K. The epitaxial structure is shown in Fig. 1. Devices were isolated with mesa process using phosphoric etchant. The ohmic electrodes were patterned by photolithography, during which the alignment marks for the subsequent electron-beam lithography were also defined. Ni/Ge/Au ohmic contacts were deposited and alloyed by rapid thermal annealing at 320℃ for 30 s. We adopted a multicap structure with a high doping concentration of $2x10^{19}$ cm^{-3} and a total thickness of 720 Å [4], in which it brought down ohmic resistances compared to single cap structure. Ohmic contact resistance and sheet resistance were 0.015 Ω mm and 25 Ω /□, respectively.

cap	$In_{0.65}GaAs$	100 Å	$2e19cm^{-3}$
	$In_{0.53}GaAs$	400 Å	$2e19cm^{-3}$
	InP	20 Å	$5e18cm^{-3}$
	$In_{0.53}GaAs$	200Å	$2e19cm^{-2}$
Etch stop	InP	60Å	undoped
Barrier	$In_{0.52}AlAs$	80Å	undoped
δ-doping	Si	-	$5e12cm^{-2}$
Spacer	$In_{0.52}AlAs$	40Å	undoped
Channel	$In_{0.53}GaAs$	20Å	undoped
	$In_{0.7}GaAs$	80Å	Undoped
	$In_{0.53}GaAs$	50 Å	Undoped
Buffer	$In_{0.52}AlAs$	5000Å	undoped
substrate	S.I. InP Sub.		undoped

Fig. 1. HEMT epitaxial layer structure with multi-cap layer.

The wide recess was realized by time-controlled wet etching using citric acid solution. The etch stopper was removed by HCl solution (HCl: phosphoric acid: H_2O=1:1:1). Using remote plasma enhanced chemical vapor deposition (RPECVD) and PECVD, we deposited a Si_3N_4 (200 Å)/ SiO_2 (200 Å)/ Si_3N_4 (200 Å) tri-layer film as a passivation layer and also as a medium for gate reduction.

3. Gate length reducing process

The initial gate stem of 0.13-um length was defined by electron beam lithography (30 keV EBMF 10.5) using ZEP (manufactured by Nippon Zeon Co.) mono-layer. After the definition of gate stem, the proposed gate length reducing process was applied to initial gate pattern. The detailed process sequences are shown in Fig. 2.

The 1st Si_3N_4 layer below ZEP mono-layer is dry etched using reactive ion etch (RIE) in SF_6/Ar gas (Fig. 2 (b)). Owing to RIE reaction between ZEP and Si_3N_4, the Si_3N_4 layer is etched away forming positive slope. Over 50 percent of total gate length reduction is realized in this process. The 2nd reactive ion etch is performed on exposed 2nd SiO_2 layer in CF_4/H_2 gas (Fig. 2 (c)). Because of polymer deposition at the corner of etched surfaces, etch rate of center is faster than it in the corner. For this reason, previous sloped profile of 1st Si_3N_4 layer is transferred to 2nd SiO_2 layer regardless of etching selectivity between Si_3N_4 and SiO_2. The final gate length is almost defined by this process. The 3rd residual Si_3N_4 layer is etched in CF_4/O_2 gas (Fig. 2 (d)). The minimum power of RIE was used to minimize damage on the semiconductor during dry etching in CF_4 gas.

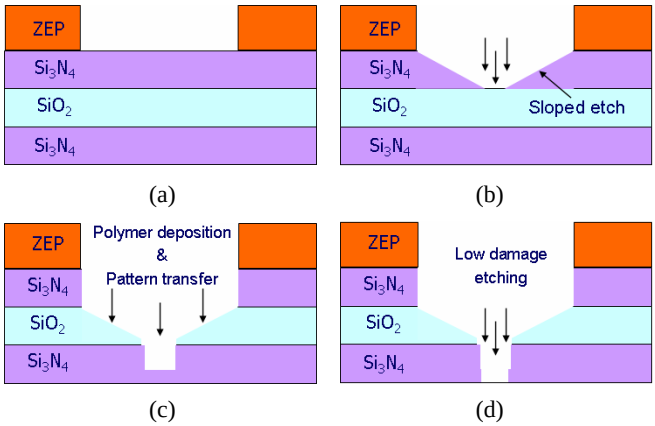
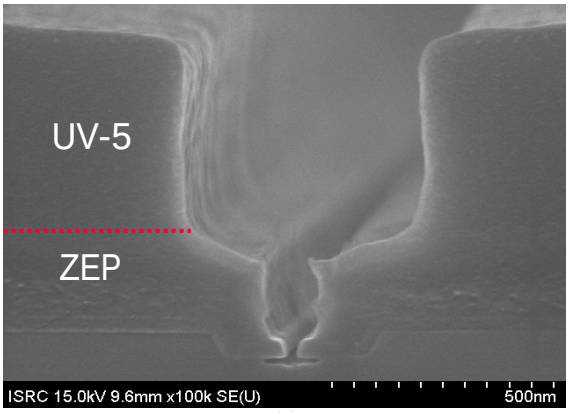
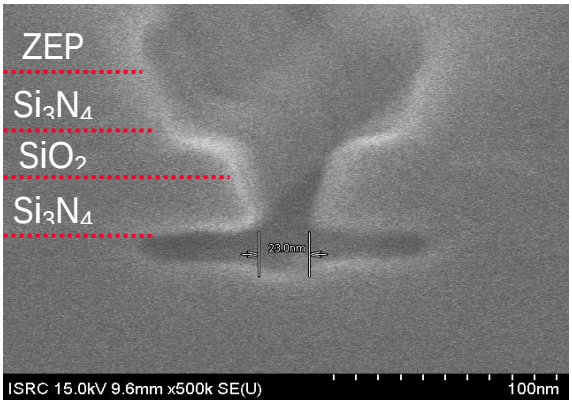


Fig. 2. Gate length reducing process (a) initial gate pattern (b) sloped etch in SF_6/Ar gas (c) pattern transfer in CF_4/H_2 gas (d) low damage etch in CF_4/O_2 gas.

After etching tri-dielectric layer, gate head was patterned using UV-5 by electron beam lithography. The completed gate pattern is shown in Fig. 3. It shows that gate stem is 130nm and length of reduced dielectric opening is as small as 23nm. The more the gate length is reduced, the harder the cap layer is recessed through the dielectric opening. To solve this problem, ultrasonically assisted recess method was applied to this study. This method was introduced in previous work [5]. The gate recess was formed by the citric acid solution with ultrasonic assist of 5 sec. and without ultrasonic assist for the rest of the time. The recess with ultrasonic assist was conducted under conditions of 35 KHz and 3.5 W in ultrasonic bath. To reduce the gate to channel distance and effective gate length and also to raise the schottky barrier height on gate, InP etch stopper under the cap layer was etched in Ar gas before gate metal evaporation. Finally, the Pt/Ti/Au gate metal was evaporated and lifted off.



(a)



(b)

Fig. 3. SEM image of T-gate pattern (a) the whole image using UV-5 for gate head (b) image focused on opening of etched dielectrics.

4. Results

The fabricated sub-30nm PHEMTs using gate length reducing process were measured on wafer for DC and RF performance. Device showed the DC characteristics of V_{th} = -0.6V, $G_{m.max}$ = 1.35 S/mm. These characteristics are shown in Fig. 4. Fig. 5 shows microwave characteristics. Unit current gain frequency f_T of 450GHz (V_{ds}=0.8V, V_{gs}=0.2V) were extrapolated from the H_{21}.

5. Conclusion

In this paper, gate length reducing process was introduced to improve RF characteristics. Using this process, the gate length was reduced from 130nm to sub-30nm. In addition, owing to lowering aspect ratio of gate stem from 150 nm: 25 nm to 150 nm: 130 nm, metal filling problem was reduced in great degree. The fabricated devices have good DC and RF performances, a transconductance of 1.35 S/mm characteristics, a maximum saturated current of 800 mA/mm and a cut off frequency f_T of 450 GHz.

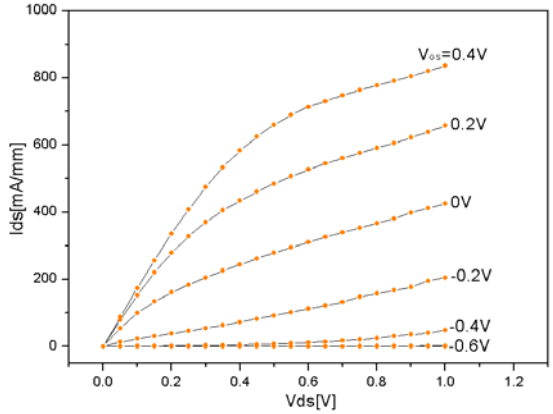


Fig. 4. DC I-V characteristics (V_{gs}=-0.6 to 0.4V with 0.2V steps).

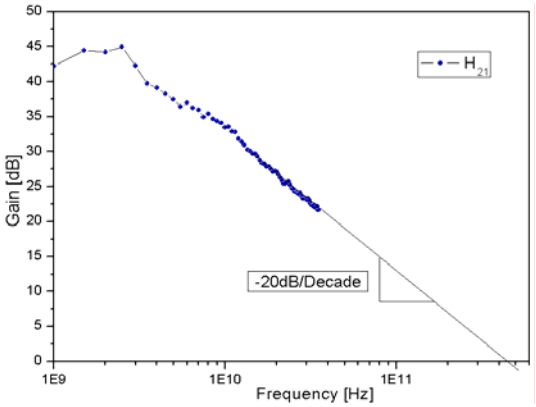


Fig. 5. RF characteristics (two fingers, W_G=25um): f_T of 450GHz (V_{gs}=0.2V, V_{ds}=0.8V) was extrapolated from H_{21} which was measured using HP8510C network analyzer.

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