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C-band GaN-FET Power Amplifiers with 160-W Output Power

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1. Introduction

There is a growing requirement for high-power and high-efficiency amplifiers in use of C-band applications, such as fixed point-to-point access systems, next-generation mobile communication systems, and satellite communication systems. Although C-band high-power amplifiers have already been developed with GaAs-based FETs [1, 2], there are still needs for the higher power with smaller size. GaN-based FETs are expected to meet these needs because of extremely high power density [3, 4]. We have developed the single-chip GaN-FET amplifiers and reported the down-sizing of 60-W amplifiers to half of the GaAs-based FET amplifiers [5] and the record continuous-wave (CW) output power of 100 W as solid-state power amplifiers [6] in C band. Although the output powers of 140 W [7] and 174W [8] are reported with multi-chip GaN-FET amplifiers under pulsed operation conditions, there are no report on over 100 W CW amplifiers.

In this work, we have designed the 2-chip GaN-FET amplifiers using the large-signal matching impedance and achieved the CW output power of 160 W at 5 GHz.

2. Amplifier design

The developed amplifier is composed of the input and output matching circuits and a couple of GaN-FET chips. The GaN-FET device is fabricated on a SiC substrate, featuring the field-modulating plates and recessed-gate structure [5]. The fabricated FET exhibits a maximum drain current of 0.7 A/mm with a pinch-off voltage of -2.1 V. The gate-drain breakdown voltage defined at -1mA/mm is 200 V. For high-power evaluation, the backside of the FET was thinned to 50μm by mechanical polishing. The gate width of the single GaN-FET chip was chosen to be 24 mm [5]. The chip size is 4.0 mm × 0.8 mm.

To design the matching circuits, we measure the optimum impedance for the 400-μm-wide FET at 5 GHz with a drain voltage of 40 V, by using an on-wafer load-pull system. For the input-matching-circuit design, the source-pull measurement is carried out under the small signal condition (input power of 0 dBm). The source impedance is scanned to find the maximum gain point, which is defined as the optimum input impedance. Its value is 8.4+25.3j Ω. The load-pull measurement is carried out under the large signal condition (input power of 24 dBm) with fixing the input impedance to the optimum value for the output-matching-circuit design.

Fig.1 shows the contour map for the output power (Pout) and the power-added efficiency (PAE). At the maximum-Pout point, the power-added efficiency drops 3 points as compared to the maximum value. On the other hand, the output power at the maximum-PAE point is as high as the maximum output power. Thus, the maximum-PAE point is determined to be the optimum output impedance. Its value is 208+87.4j Ω. Fig.2 shows the power performance for the 400-μm-wide device with the optimum input and output impedance. The saturated output power of 35.2 dBm, the linear gain of 13.5dB and the power-added efficiency of 48% are obtained with a drain voltage of 40 V.

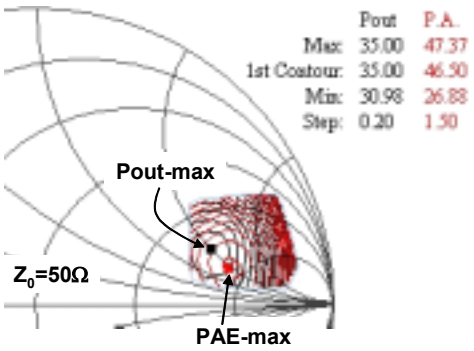

Fig.1 Contour map for the output power (black lines) and power-added efficiency (red lines).

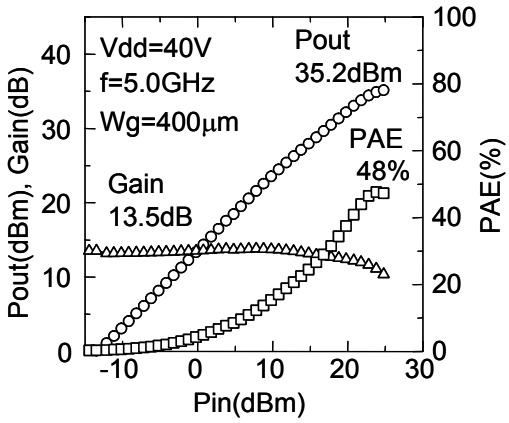

Fig.2 Output power, linear gain and power-added efficiency for 400-μm-wide device as a function of input power.

Fig.3 shows the equivalent circuit of the developed amplifier. The optimum input and output impedances for the 400-μm-wide device are scaled to those for the 24-mm-wide device. To reduce the impedance transformation ratio, we use single-stage LC low-pass filters and a divider composed of single-stage quarter-wave transformers for the input matching circuit and a combiner composed of 2-stage quarter-wavelength transformers for the output matching circuit. The divider and the combiner are formed on a single alumina substrate to avoid the inter-substrate losses.

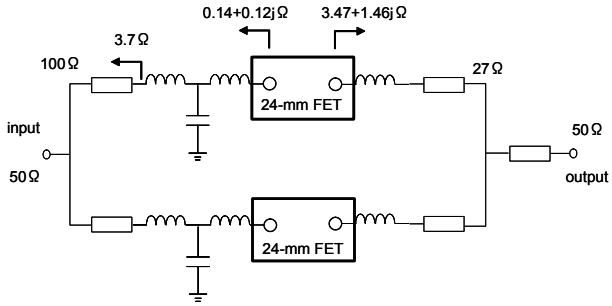

Fig.3 Equivalent circuit for 2-chip GaN-FET power amplifier.

3. Amplifier performance

Fig.4 shows the measured small-signal gain, input and output return losses for the developed 2-chip GaN-FET amplifier with a drain voltage of 40V. A small-signal gain of 8 dB is obtained at a frequency of 5.0 GHz. The input and output return losses are -14 and -11 dB, respectively. The CW power performance is examined at a frequency of 5.0 GHz. Fig. 5 shows the output power, the gain and power-added efficiency as a function of the input power with a drain voltage of 50 V. The developed GaN-FET amplifier demonstrates a saturated output power of 161 W with a 10.7 dB linear gain and a 34.2% power-added efficiency. To the best of our knowledge, this is the highest CW output power achieved from solid-state power amplifiers at this frequency band.

4. Conclusion

A C-band high-power amplifier is successfully developed with 2-chip 24-mm-wide GaN-FETs. At 5.0GHz, the fabricated GaN-FET amplifier delivers a 161 W CW output power with 10.7 dB linear gain and 34.2% power-added efficiency with a drain voltage of 50 V. To the best of our knowledge, this is the highest CW output power achieved from a solid-state power amplifier at C-band.

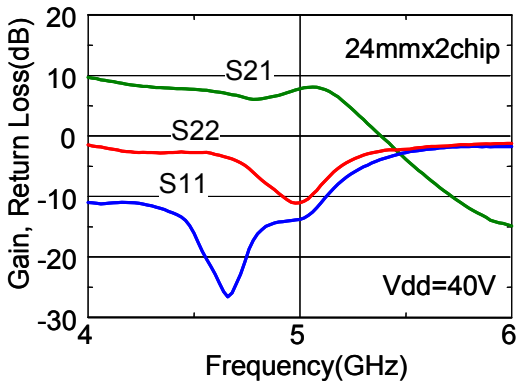

Fig.4 Small-signal characteristics for 2-chip GaN-FET amplifier

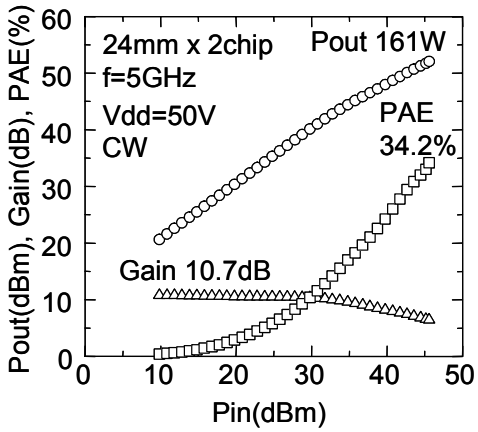

Fig.5 Output power, linear gain and power-added efficiency for 2-chip GaN-FET amplifier as a function of input power.

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