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Electrical and Optical Properties of an n-Channel GaN Schottky Barrier MISFET

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I. Introduction

GaN and its alloys based electron devices are very promising material for high frequency power operation under the harsh environments, since they have large direct bandgap and high electron saturation velocity. AlGaN/GaN HFET has been considered as a strong candidate for commercial application [1]. But MESFET type structure suffers from the gate leakage current and the current collapse. While the MOSFET provides the normally-off mode transistor action with much lower gate leakage current, which are preferred for high speed logic and power devices with simple driving circuit and less power consumption. However, it is not easy to grow a high quality p-GaN layer, which has been typically doped with Mg and exhibited low mobility less than 10 cm^2/Vs.

An enhancement type n-channel GaN MOSFET was fabricated by Si^+ ion implantation for the source/drain region, which exhibited no drain current saturation [2]. A normally-off GaN MOSFET was reported but with a leakage current of $2x10^{-7}$A, high threshold voltage of 2.7 V [3]. Depletion type GaN MOSFETs have been fabricated using different gate dielectrics [4,5,6].

In this work, we investigated the electrical properties and photo responsive characteristics of the fabricated n-channel GaN MISFET with schottky barrier source/drain, which is very attractive because it excludes the ion implantation and high temperature activation [1]. In addition, it can alleviate the DIBL (drain induced barrier lowering) problem in short channel device [7].

II. Fabrication of GaN SB-MISFET

Fig. 1 shows a schematic cross section (a), fabrication process flow (b) and operation principle (c) of the proposed schottky barrier MISFET. We fabricated the SB-MISFET on the high quality p-GaN epitaxial layer grown by MOCVD on (111) oriented n-type silicon substrate. The grown 700 nm thick p-GaN layer had a hole concentration of $2.1x10^{17}$ cm^{-3} a hole mobility of 228 cm^2/Vs [8]. The schottky barrier source and drain were formed on the p-GaN layer by 100 nm thick aluminum whose work-function of 4.3 eV was close to the electron affinity of GaN. The threshold voltage and the drain current depend directly on the work-function of gate metal. Si_3N_4 (150 nm) was deposited for gate dielectric using PECVD at 300 ^oC. Finally, 200 nm thick gold was deposited for gate metallization. The electrical and optical properties of SB-MISFETs were characterized using HP4155 semiconductor parameter analyzer and UV spectral photoresponse system with a 150 W Xenon arc lamp. In selection of gate dielectric, good surface passivation is required to reduce the interface states between gate dielectric and GaN surface.

III. Results and Discussions

Fig. 2 is one of the photoluminescence (PL) spectrum of the p-type GaN epitaxial layer, which is grown on the silicon substrate and used to fabricate the device, exhibiting a significant peak at 365 nm wavelength and broad intensities at the longer wavelength region, probably attributed to the deep traps in GaN layer. The inset figure shows a cross-sectional schematic of the epitaxial layers. Fig. 3 shows the typical output characteristics of the fabricated n-channel GaN SB-MISFET with 10 um gate length and 100 um gate width. Maximum drain current is over 1 uA/mm and the maximum transconductance is 0.4 uS/mm as shown in the I_{DS}-V_{GS} characteristic at high drain bias of 10 V in Fig.4. It has a threshold voltage of 2.7 V and a sub-threshold slope of 1.6 V/dec from the low drain bias voltage of 0.5 V. And the off-current of the fabricated MISFET is 0.2 nA/mm, which is much smaller than the typical GaN HFET [9] in Fig. 5.

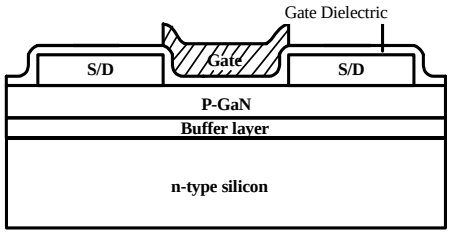
Fig. 6. The spectral responsivity of the fabricated SB-MISFET at V_{DS}=5V and V_{GS}=0 V. The measured cutoff wavelength was about 365 nm and the highest UV/visible rejection ratio was about 100. The reason of the weak rejection ratio for the device with very low off-current is possibly the deep trap levels in the p-type GaN epitaxial layer and the interface or surface states near the gate stack and/or the source/drain contacts on p-type GaN layer. They will be the origin of the low energy photon absorption, which may finally contribute to the photo-responsive current over the cutoff wavelength region.

From Fig. 7, we find a significant hysteresis of the drain electrical current, which is another exposition of the instable quality of the interfaces. Because of the deep trap levels in the GaN epitaxial layer and/or interface between the source/drain Schottky metal and GaN surface, there is 1V hysteresis between increasing and decreasing sweep of the source-drain bias. So there can be significant improvement is expected if proper passivation and better interface quality is ensured during the process.

IV. Conclusions

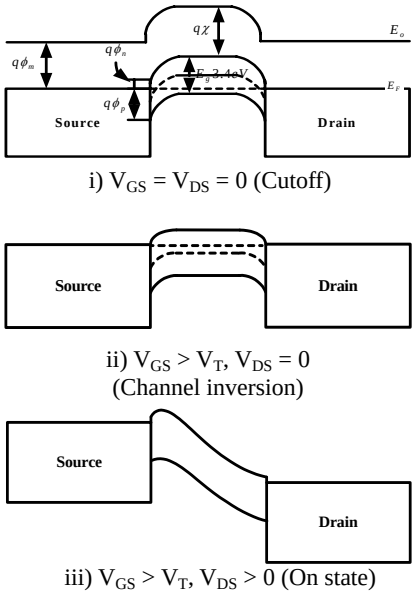
We investigate the electrical properties and photo responsive characteristics of SB-MISFET on the high quality p-type GaN layer grown on silicon substrate. The fabricated devices exhibited a threshold voltage of 2.7 V, the maximum drain current of over 1 uA/mm and the maximum transconductance of 0.4 uS/mm at V_{GS} of 10 V, and drain leakage current density of less than 1 nA/mm^2. Under illumination, the cutoff wavelength was 365 nm, and the UV/visible rejection ratio about 100 at V_{DS} = 5 V and V_{GS} = 0 V. If the growth condition and fabrication process condition are optimized, the SB-MISFET will be one of fascinating candidates for GaN power and logic integrated circuit applications.

Reference
[1] H. Yu et. al., IEEE EDL, Vol. 26, No. 5, p. 283, 2005
[2] A. Kinoshita et. al., 2005 Symp. VLSI Tech., p. 158, 2005
[3] Y. Irokawa et. al., Appl. Phys. Lett., Vol. 84, No. 15, p. 2919, 2004
[4] K. Matocha et. al., IEEE EDL, Vol. 52, No. 1, p. 6, 2005
[5] S. Binari et. al., Proc. Electrochem. Soc., Vol. 95-21, p. 136
[6] F. Ren et. al., Solid-State Electron., Vol. 43, p. 1817, 1999
[7] P. Chen et. al., Proc. Mater. Res. Soc., Vol. 622, p. T2.9.1, 2000
[8] A. Gurskii et.al., Phys. Stat. Sol.(c), Vol.0, No.1, p.425-429, 2002
[9] N. Ikeda et.al., Proceedings of ISPSD & ICs. p.369-372. 2004



(a)

(b)



(c)

Fig. 1. The proposed schottky barrier MOSFET; structure (a), process flow (b), and its operation modes (c)

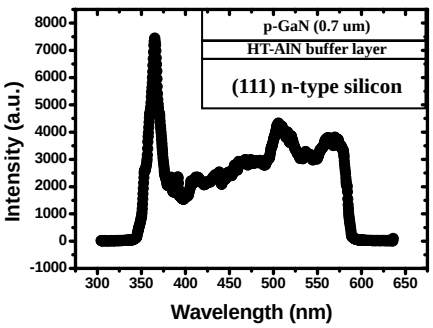


Fig. 2. photoluminescence spectrum of the epitaxial layer used in this work (inset shows the p-GaN epitaxial structure grown on the silicon substrate)

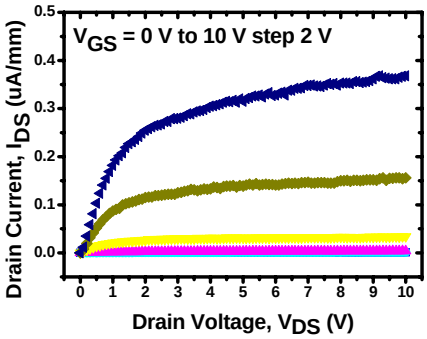


Fig. 3. Output characteristics of the fabricated SB-MISFET with W/L=100/10 um

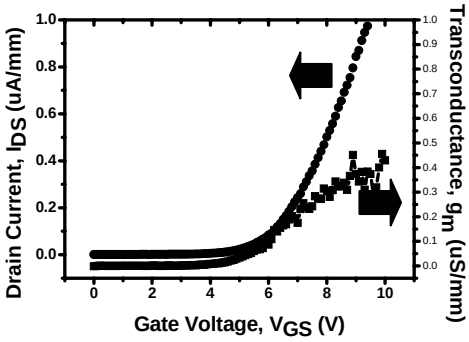


Fig. 4. I_{DS} -V_{GS} characteristics of the fabricated SB-MISFET with W/L=100/10 um at V_{DS}=10 V

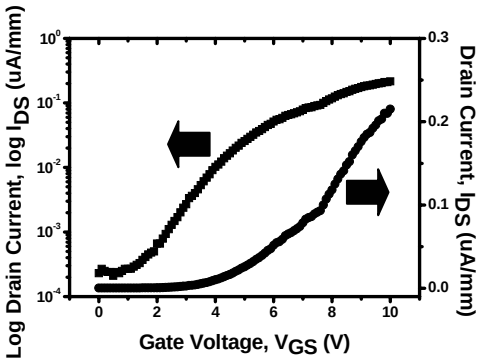


Fig. 5. I_{DS} -V_{GS} characteristics of the fabricated SB-MISFET with W/L=100/10 um at V_{DS}=0.5 V

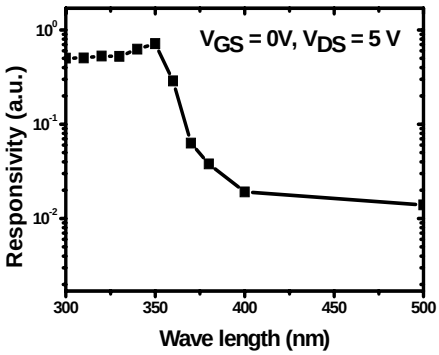


Fig. 6. The spectral responsivity of the fabricated SB-MISFET with W/L=100/10 um at V_{DS}=5V and V_{GS}=0 V

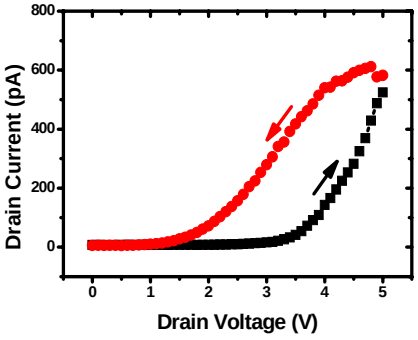


Fig. 7. I_{DS} -V_{DS} characteristics between source and drain electrode at swept from 0 V via 5 V back to 0 V