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Self-Heating Induced Germanium Outdiffusion and Non-Local Channel Degradation in the Strained-Si/SiGe N-MOSFET subjected to Channel Hot-Electron Stress

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Abstract

We report evidence of *Ge outdiffusion* and severe *non-local* channel degradation in strained-Si/SiGe N-MOSFETs (channel width $W > 0.5$ μm) subjected to channel hot-electron stress. Analysis shows that the high channel temperature (~700-750°C at $V_g = V_d = 2.7$V stress condition) arising from significant self-heating in these devices is primarily responsible. On the other hand, the channel temperature of the bulk-Si control device is only ~150°C at the same stress condition. AC stressing of the strained-Si device yields slightly lower channel degradation due to reduced self-heating. Besides increased impact ionization, the induction of other failure mechanisms by self-heating pose further challenge to the reliability of the strained-Si devices.

I. Introduction

The strained-Si/SiGe technology can significantly enhance the performance margin achieved through downscaling of the conventional bulk-Si MOSFET[1,2]. However, concerns on strain relaxation and Ge outdiffusion pose important integration challenges[3,4]. To-date, studies are mainly focused on process-induced issues, and reliability studies are limited[5-7]. Because of the much lower thermal conductivity of the underlying SiGe layer, the strained-Si device is known to suffer significant self-heating. In this work, we report observations of hot-electron stress induced Ge outdiffusion and the associated non-local channel degradation in the strained-Si N-MOSFET.

II. Device Fabrication

Strained-Si N-MOSFETs on relaxed SiGe virtual substrate with 15% and 20% Ge concentration were fabricated using a state-of-the-art CMOS process. The final thickness of the strained-Si layer is ~15nm and the underlying SiGe layer is ~1 μm thick. Thermal budget was limited by replacing STI sidewall and implant screen oxides by low temperature CVD-TEOS oxide. Bulk-Si devices were fabricated using an exact processing sequence. Drain current enhancement of ~15% was achieved in the 20% Ge strained-Si device, as evident in Fig. 1.

III. Results and Discussion

(A) Measurement of Channel Temperature

A phenomenological model[8] was used to extract the channel temperature ΔT_{ch} (minus the chuck temperature) of the strained-Si (SS) device. The algorithm is summarized in Table 1. Fig. 2 shows substantial self-heating in the SS devices ($W > 0.5$μm)[9], yielding ΔT_{ch} ~700-750°C at the nominal stress condition of $V_g = V_d = 2.7$V. The same approach applied to the bulk-Si control device gives ΔT_{ch} ~150°C at the specific stress bias, in agreement with previous report[10]. With a high channel temperature in the 800°C range, other failure mechanisms are induced by channel hot-electron stressing as described below.

(B) Channel Hot-Electron Stress Induced Ge Outdiffusion

The high channel temperature of the SS device biased at the nominal stressing condition can in fact induce Ge outdiffusion from the underlying SiGe layer. This prediction is confirmed in Fig. 3-4. Using energy dispersive *x*-ray spectrometry with a probe size of ~1 nm, Ge concentration (C_{Ge}) at 3 locations (gate edges at the drain and source, and channel region) in a 20% Ge SS device (Fig. 3(a)), subjected to $V_g = V_d = 2.7$ V stress, were measured and compared to those obtained in a fresh device. The variation of C_{Ge} as a function of depth into the composite strained-Si/SiGe layer of a fresh SS device is shown in Fig. 3(b). As expected from a well controlled thermal budget, C_{Ge} in the strained-Si layer is low (< 2%) and rises steadily towards 20% in the relaxed SiGe buffer. Fig. 3(c) shows C_{Ge} variation at $T_{Si} = 5$ nm. Fig. 3(d) depicts the threshold voltage (V_{th}^o) distribution of fresh SS devices. The small variation in V_{th}^o (~12 mV) of the fresh SS devices implies that C_{Ge} in the strained-Si layer does not vary significantly among the fresh SS devices. On the other hand, Fig. 4(a) shows that C_{Ge} in the channel region is doubled after hot-electron stress. Fig. 4(b) shows the statistical spread in $\Delta C_{Ge}/C_{Ge}^o$ obtained from numerous devices stressed at the same condition, confirming that maximum fractional increase in C_{Ge} occurs within the channel region.

(C) Non-Local Channel Degradation

The significant outdiffusion of Ge from the underlying SiGe layer towards the strained-Si layer during channel hot-electron stress corroborates the observation of severe channel degradation in the device. The finding of non-local hot-electron induced damage is illustrated in Fig. 5 where the linear I_d degradation extracted at low (high) V_g probes damage situated in the channel (gate edge) region[11]. The control device exhibits classical degradation behavior; $|\Delta I_d/I_d^o|$ ($@V_g \approx V_{th}^o$) is ~1% in the initial stress stage, i.e. hot-electron induced damage is localized near the drain edge, but extends gradually into the channel region as time increases[11]. On the other hand, substantial degradation in the linear I_d of the SS device is apparent even in the initial stage. For the 15% Ge SS device, $|\Delta I_d/I_d^o|$ ($@V_g \approx V_{th}^o$) ~35% after 1s stress, and the fractional degradation is doubled for the 20% Ge SS device. The shift in threshold voltage (ΔV_{th}) and charge pumping current (ΔI_{cp}) data in Fig. 6 corroborate the linear I_d degradation pattern of Fig. 5, confirming a much greater extent of spatial damage in the SS devices.

The severe channel degradation of the SS device at very short stress time implies that Si-SiO_2 interface and oxide damage in the device is not dominated by drain-side hot-electron injection and points to the role of non-local mechanisms. In this case, self-heating is believed to have induced the generation of excess hot electrons non-locally via lattice interaction, leading to the degradation of nearly the entire channel region in a short stress interval. Fig. 7 compares the impact ionization rate (I_b/I_d) of the SS and control devices. A significant enhancement in I_b/I_d , especially in the high V_g regime[12], is apparent in the former.

As evident in Fig. 2, channel temperature rises significantly in devices with $W > 0.5$ μm. To verify the role of self-heating, we investigated the degradation kinetics of the $W = 0.5$ μm devices. In this case, the stress induced change in $|\Delta I_d/I_d^o|$ ($@V_g \approx V_{th}^o$) reverts to classical behavior. As depicted in Fig. 8(a), $|\Delta I_d/I_d^o|$ ($@V_g \approx V_{th}^o$) of the narrow SS devices falls well below 10% in the initial stress stage and increases progressively with time. The data for ΔV_{th} and ΔI_{cp} in Fig. 8(b) and (c) further corroborate the above discussion.

(D) AC Gate Stress Induced Degradation

Fig. 9 shows the $|\Delta I_d/I_d^o|$ data obtained from ac gate stress, with the stress duty cycle D_{str} as the parameter. For the control device, "universal" degradation curves result when $|\Delta I_d/I_d^o|$ is plotted against the effective stress time $T_{str(eff)}$, defined by the actual stress interval T_{str} x D_{str}. The relatively low stress bias would not result in significant hot-hole injection associated with the pulse transient period[13], which is responsible for the increased ac degradation previously reported. With the selected pulse transition time (50ns) being much smaller than the smallest stress duty cycle for the given frequency, the overall degradation is dominated by the ON cycle, i.e. $V_g = V_d$. However, this is not the case for the SS devices. Reduced degradation is apparent with decrease in the stress duty cycle; reduction is particularly significant for the $|\Delta I_d/I_d^o|$ ($@V_g \approx V_{th}^o$) parameter, confirming the role of device self-heating on non-local degradation.

IV. Summary

In this work, we report first evidence of Ge outdiffusion and severe non-local channel degradation induced by channel hot-electron stressing of the strained-Si/SiGe N-MOSFET. It is shown that self-heating is the main driving force, and channel temperature could reach the ~700-750°C range for the devices studied, at stress conditions commonly applied to the bulk-Si device.

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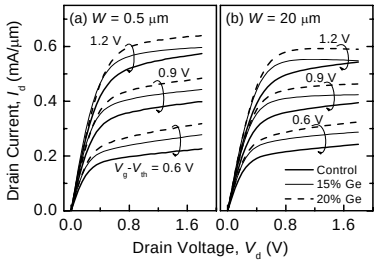
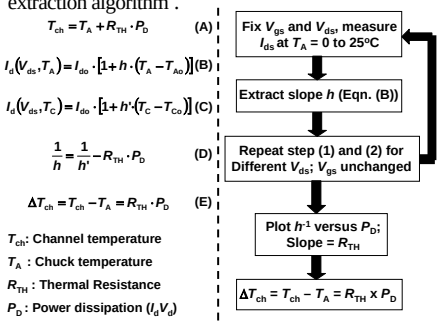


Fig. 1: I_d–V_d of strained-Si and bulk-Si N-MOSFETs at selected gate overdrives. L = 0.18 μm; T_{ox} = 3 nm.

Table 1: Flowchart depicting the channel temperature extraction algorithm[8].



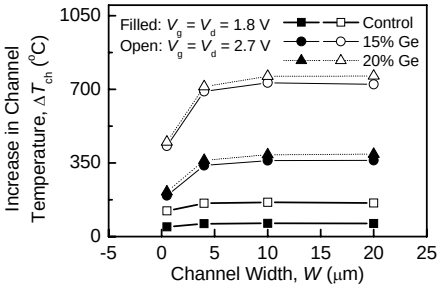
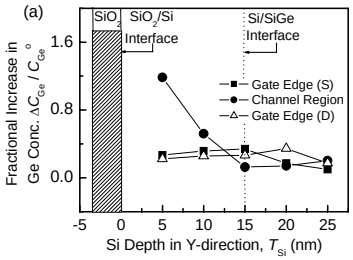


Fig. 2: Increase in channel temperature ΔT_{ch} as a function of channel width W for strained-Si and bulk-Si N-MOSFETs biased at $V_g = V_d$ = 1.8 V and $V_g = V_d$ = 2.7V (stress condition). Chuck temperature = 25°C



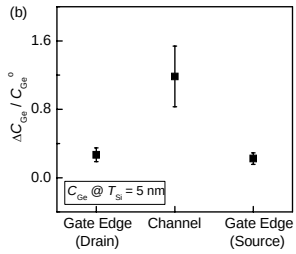


Fig. 4: (a) Fractional increase in Ge concentration $\Delta C_{Ge}/C_{Ge}^o$ at the gate edges and channel region as a function of depth T_{Si}. The strained-Si N-MOSFETs (W = 20 μm) were stressed at $V_g = V_d$ = 2.7 V for 7×10^4 s. (b) Statistical variation of $\Delta C_{Ge} / C_{Ge}^o$ extracted at T_{Si} = 5 nm.

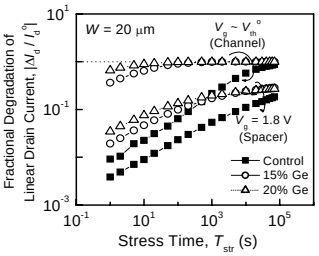


Fig. 5: Fractional degradation in linear I_d, $|\Delta I_d/I_d^o|$ extracted at $V_g \approx V_{th}^o$ (V_{th} of fresh device) and V_g = 1.8 V; V_d = 0.1 V. The former probes hot-electron induced damage in the channel region and the latter probes damage at the gate edge (drain)[11].

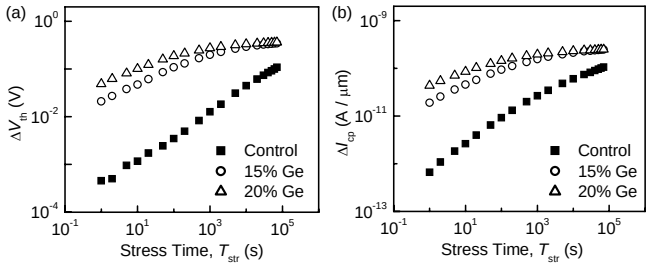


Fig. 6: (a) Threshold voltage shift ΔV_{th} and (b) charge pumping current increase ΔI_{cp} for the same strained-Si N-MOSFET as that of Fig. 5.

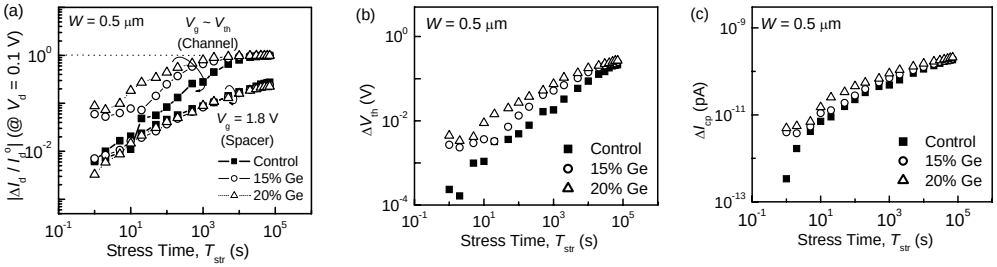


Fig. 8: (a) Fractional degradation in linear I_d, $|\Delta I_d/I_d^o|$ as a function of stress time for narrow width devices (W = 0.5 μm). The corresponding (b) ΔV_{th} and (c) ΔI_{cp} data.

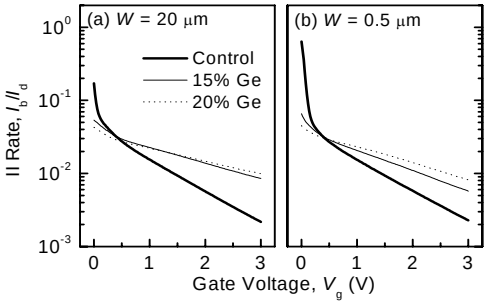


Fig. 7: Impact ionization (II) rate I_b/I_d (I_b - substrate current) as a function of gate voltage V_g showing significant generation of excess hot carriers in the strained-Si N-MOSFETs in the high V_g regime.

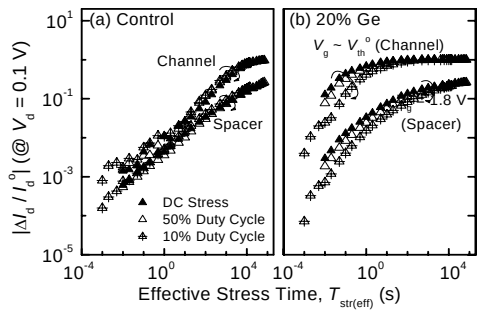


Fig. 9: Fractional degradation in linear I_d, $|\Delta I_d/I_d^o|$ of (a) bulk-Si and (b) strained-Si N-MOSFETs subjected to dc and ac gate stress (varying stress duty cycles D_{str}), as a function of effective stress time $T_{str(eff)}$ (= T_{str} x D_{str}).

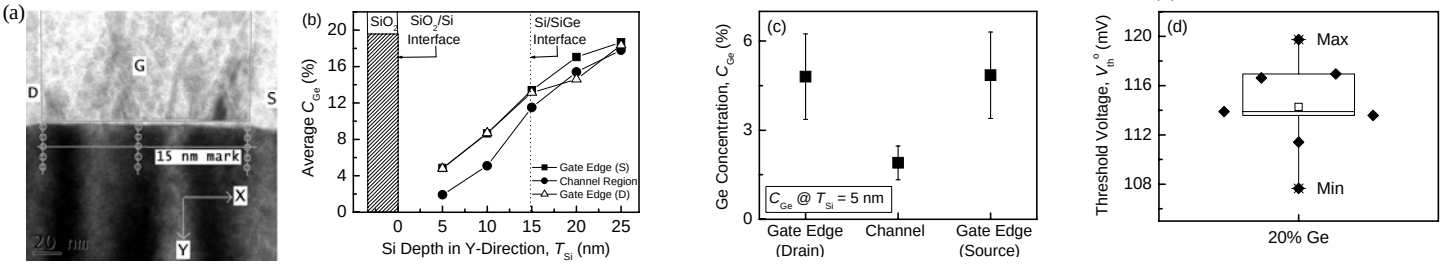


Fig. 3: (a) TEM cross-section of 20% Ge strained-Si N-MOSFET (W = 20 μm); open circles denote positions at which Ge concentrations are measured; horizontal demarcates the strained-Si (thickness 15 nm)/SiGe interface. (b) Variation of Ge concentration C_{Ge} as a function of depth T_{Si} at the gate edges and channel region of fresh strained-Si N-MOSFETs. (c) Statistical variation of C_{Ge} extracted at T_{Si} = 5 nm. (d) Threshold voltage variation of fresh strained-Si N-MOSFETs.