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Ni(alloy)-germanosilicide contact technology for $Si_{1-x}Ge_x$ (x=0.20-0.5) junctions

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Abstract Ni germanosilicide contact technology alloying with 5-10% atomic percentage of Pt, Pd and Pt-Pd has been found to exhibit superior morphology stability and interface quality at high temperature. In addition, with alloying, low resistivity Ni-mono-germanosilicide is promoted at an annealing temperature as low as 200°C without compromising its electrical performance, thus widening the processing temperature window.

Introduction Ni silicide technology has been used for sub-90nm Si-based technologies because of its low formation temperature and less silicon comsumption. Lee *et al.*[1] reported Ni(Pt) technology for advanced Si CMOS and Öztürk *et al.* reported Ni-germanosilicide technology for advanced SiGe source/drain (S/D) junctions[2]. In this paper, we report Ni(5-10 at.% Pt, Pd, Pt-Pd)-germanosilicide contact technology for $Si_{1-x}Ge_x$ (x=0.2-0.3 and 0.5) source/drain junctions.

Effect of alloying on morphology and phase transformation A series of experiments were performed to obtain the optimal atomic concentration of Pt and Pd alloy in Ni on undoped and doped $Si_{1-x}Ge_x$(x=0.2-0.3) for the best material properties of the formed germanosilicide[3,4]. It has been found that a 10% Pt or 5% Pd atomic percentage gives the best material and thermal stability performance. Fig. 1 shows the electrical sheet resistance of various Ni alloying systems on $Si_{0.75}Ge_{0.25}$ substrate. A dramatic increase in the sheet resistance of *pure* Ni-germanosilicide occurs after 600°C, attributed to severe film agglomeration (revealed by SEM but not shown here) and Ge out-diffusion. With Pt incorporated, the low sheet resistance, including Ni(Pt-Pd), can be maintained up to an annealing temperature as high as 700°C, enlarging the process temperature window by ~100°C as compared to that of the pure Ni alloy system. This is due to a stronger Pt-Si(Ge) bond and less surface diffusion of Ni(Pt) films[3]. Even for Ni(Pd), it still shows a better performance than the pure Ni. Similar improvement in the sheet resistance, attributed to early *mono*-germanosilicide, is seen for all the alloying systems at low annealing temperature of 200°C. The micro-Raman results shown in Fig. 2 confirms that the Ni(Pt) and Ni(Pt-Pd) alloy suppress Ge out-diffusion at high annealing temperature, as proven by the different shapes of the $NiSi_{1-x}Ge_x$ peak. Fig. 3 shows the variation of the Ni $2p^3$ binding energy as a function of annealing temperature for the Ni and Ni(alloy) systems collected by an in *in-situ* XPS system i.e., analyze the phase while annealing without breaking vacuum). The addition of Pt or Pd has promoted the *mono*-germanosilicide (with x same as the substrate) formation at 200°C, consistent with the sheet resistance results in Fig. 1. As shown in Fig. 4(a), Ni(Pd) and Ni(Pt-Pd) provide superior metal/semiconductor interface, in particular the Pd alloy is able to provide highly textured film[4], in agreement with the x-ray diffraction frame results shown in Fig. 4(b). Hence, in summary Ni(alloy) has the following advantages: 1) 5-10 at.% of Pt or Pd alloy in Ni promotes *mono*-germanosilicide formation as early as 200°C, 2) Pt suppresses Ge out-diffusion and agglomeration at high temperature up to 700°C, and 3) Pd provides excellent interface quality, important for junction leakage, from 200 to 600°C. The ternary alloy combining a 10 at.% Pt and 5 at%. Pd takes the advantages of both Pt and Pd alloying, providing an enlarged processing window and good interface quality of low resistivity *mono*-germanosilicide from 200-700°C (Fig. 5).

Ni(alloy)-germanosilicided junction The electrical performance of the Ni(alloy) systems on p^+-n $Si_{0.75}Ge_{0.25}$ and $Si_{0.5}Ge_{0.5}$ diodes (see Table 1 for the experimental details) was studied. Fig. 6(a) shows that the ideality factor (n) and saturation current (I_0) decrease with increasing Pt concentration even at a germanosilicide annealing of 600°C (for 10 at.% Pt). For the Ni(Pd) samples, better n and I_0 are only obtained at lower annealing temperatures of 300 to 500ºC. Fig. 6(b) shows that a better leakage performance is achieved with the Ni(Pt) alloy as compared with that of the pure Ni germanosilicide, especially at higher annealing temperature of 500 and 600ºC (i.e., due to a better film morphology shown in Fig. 2). Ni(Pd) shows a similar improvement up to only 500ºC, consistent with the excellent texture and interface data in Fig. 4(a). High Ge concentration $Si_{0.5}Ge_{0.5}$ substrate was also used for junction leakage study. In order to ensure sufficient *implanted* boron atoms are activated without incurring Ge outdiffusion, an optimal RTA activation temperature of 700ºC was chosen for the *implanted* boron as maximum forward current drive can be obtained. Even for 50% Ge concentration, Ni(alloy) is still able to improve the mono-Ni-germanosilicide film morphology as shown in the sheet resistance results (Fig. 7), I_0 (Fig. 8(a)) and junction leakage (Fig. 8(b)) as compared to that of *pure* Ni. This is consistent with the results obtained from the $Si_{0.75}Ge_{0.25}$ substrates.

Summary Ni(alloy)-germanosilicide technology employing Pt, Pd and Pt-Pd as the alloy has been shown to be a better contact technology for $Si_{1-x}Ge_x$ substrates (with x up to 50%). As Pt alloy is able to reduce the releasing rate of Ni into Si[5], and stronger Pt-Si is able to minimize surface diffusion[3], Ni(alloy) can minimize process integration issues as such void encroachment beneath spacer and bridging between gate to S/D and along STI. Hence, Ni(alloy)-germanosilicide technology is a promising candidate for future *low thermal budget* nano-scale CMOS technologies.

Reference [1] P.S. Lee *et al.,* IEEE EDL,22,568(2001). [2] M.C. Öztürk, *et al.,* IEDM Tech. Dig. 957(2002). [3] L.J. Jin *et al.,* JAP, 98, 033520(2005). [4] L.J. Jin *et al.*, JAP, 97, 104917(2005). [5] P.S. Lee *et al,* SSC,128, 325(2003).

Table 1: Process flow for pn diode fabrication.

#	Steps
1	Clean (100:10HF+Piranha)
2	Isolation /Coat PR
3	Pattern/ Develop/Hard bake
4	Etch exposed SiO_2
5	Remove PR using Acetone
6	Implantation for pn diode Dos:4E15cm^{-2}
7	Dopant activation
8	Salicide process
9	Etchback unreacted metal
10	Backside metal evaporation

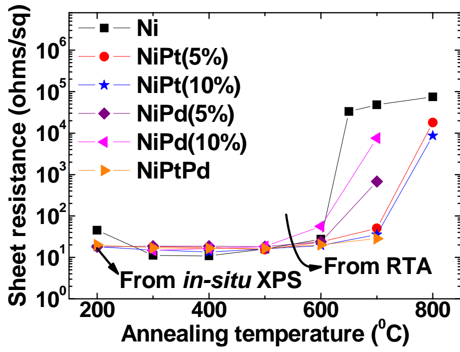


Fig. 1: Sheet resistance as a function of the annealing temperature for different Ni alloy on $Si_{0.75}Ge_{0.25}$ substrate. A 10 at. % Pt and 5 at. % Pd were used for the Ni(Pt-Pd) ternary system.

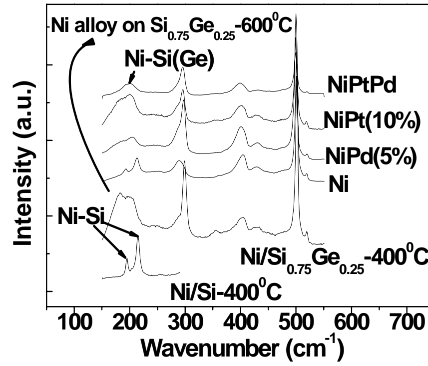


Fig. 2: Raman spectra of Ni alloy on $Si_{0.75}Ge_{0.25}$ substrate annealed at 600°C. The samples of Ni on Si and $Si_{0.75}Ge_{0.25}$ annealed at 400°C are included for comparison.

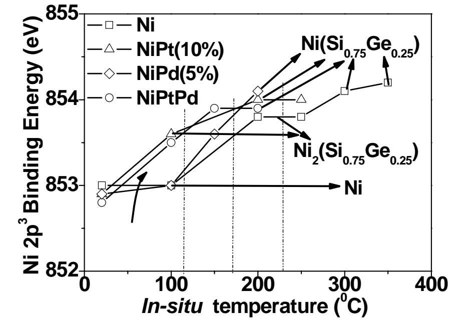
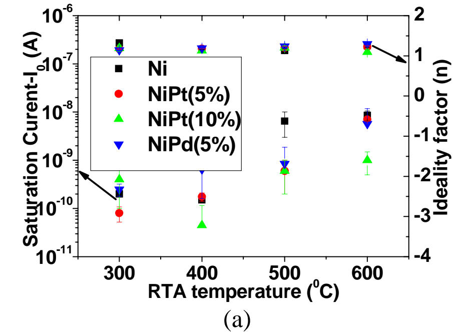
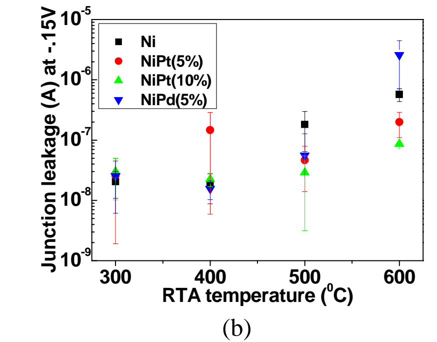


Fig. 3: Ni $2p^3$ binding energy obtained by XPS versus *in-situ* annealing temperature for different Ni alloy systems on $Si_{0.75}Ge_{0.25}$.



(a)



(b)

Fig. 6: (a) Saturation current and ideality factor and (b) junction leakage as a function of RTA temperature for Ni(alloy)-germanosilicided p^+-n junctions on $Si_{0.75}Ge_{0.25}$ (diode area=600x600µm).

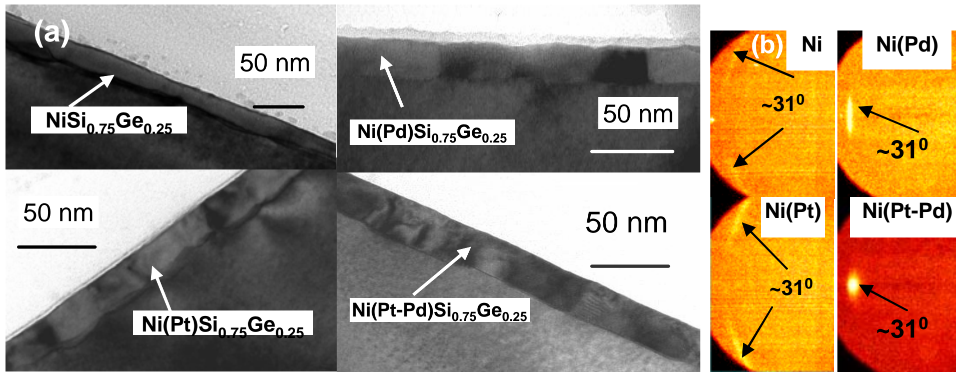


Fig. 4: (a) TEM images and (b) XRD frames of Ni(alloy)-$Si_{0.75}Ge_{0.25}$ annealed at 400°C.

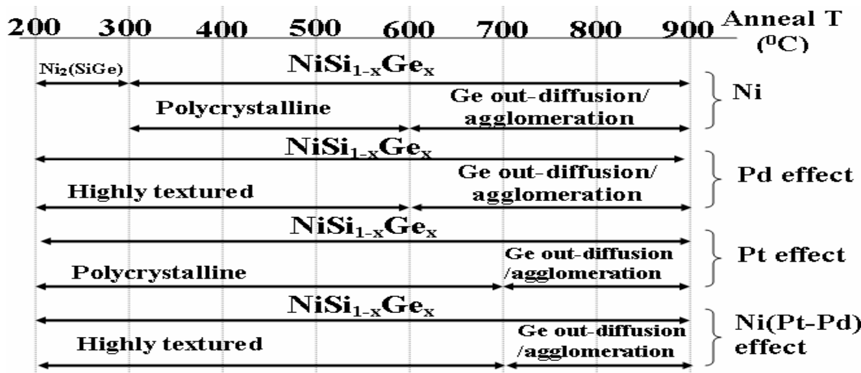


Fig. 5: Comparison of processing temperature window for different Ni(alloy) systems on $Si_{0.75}Ge_{0.25}$ substrate.

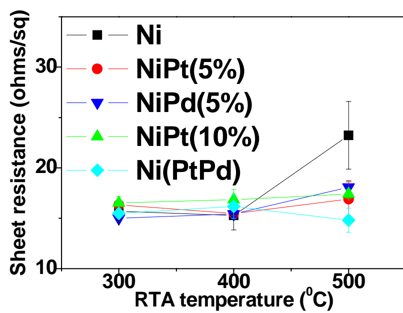
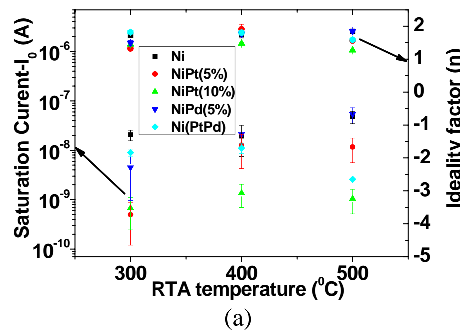
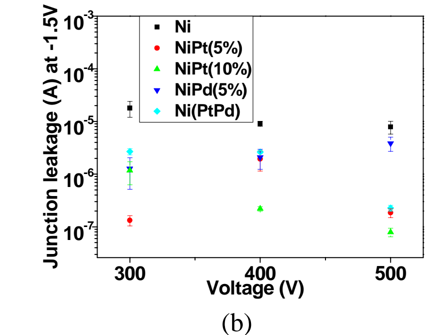


Fig. 7 Sheet resistance as a function of RTA temperature for Ni(alloy) systems on $Si_{0.5}Ge_{0.5}$ substrates.



(a)



(b)

Fig. 8: (a) Summary of I_0 and n and (b) junction leakage for Ni(alloy)-germanosilicided p^+-n junctions on $Si_{0.5}Ge_{0.5}$ substrates (diode area=220x220µm).