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Impacts of Si Crystal Orientation on NiSi Silicided Junction Leakage Induced by Anisotropic Ni Migration

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1. Introduction

For sheet resistance reduction of ever shallowing S/D junctions, NiSi is now utilized as a primary SALICIDE material due to its small Si consumption and low formation temperature [1]. At the same time, in an effort to maximize the current drivability, growing attention is now directed toward CMOS integration over a hybrid orientation substrate, forming nFETs and pFETs on Si(100) and Si(110) surfaces, respectively [2]. Thus, in order to gauge viability and practicability of this new option, impacts of the Si crystal orientation on the leakage of NiSi silicided shallow junctions must be thoroughly investigated. Regarding thin NiSi films formed on Si(100), an in-depth study has revealed thermal instability of thin NiSi and associated substantial leakage generation on shallow junctions even during thermal processing at 500^{o}C (i.e., a typical temperature for interlayer formation by CVD)[3]. Since such low temperature intolerance significantly impairs device manufacturability, clarification of the thermal instability is urgently required also for NiSi on Si(110). Nonetheless, regarding NiSi on Si(110), the desired basic and systematic investigation of thermal instability and leakage generation has never been conducted. Hence, the present paper reports a sensitive and comparative study of crystal orientation dependency of annealing effects on NiSi induced junction leakage. For the first time, coordinated experiments secured clear evidence of anisotropic migration of Ni clusters in the Si crystal.

2. NiSi Formation on Damage-Free Junction

Fig.1 illustrates the procedure for damage-free junction formation employed in this study. The details of the fabrication will be found in ref. [3]. After formation of a virtually flat p-well over 8-inch, p-type, CZ, Si(100) or Si(110) wafers, a junction region is delineated by RIE-etching a SiN film and wet-etching an underlying TEOS film, avoiding plasma damage to the substrate (Fig.1-a). Subsequently, AsSG film is deposited and annealed to form an n+ region by solid phase diffusion into the opening defined above (Fig.1-b). By adjusting the annealing time and temperature, n+/p junctions with various depths can be readily obtained [3]. After AsSG removal by wet etching, SiN sidewalls are formed to guard the periphery (Fig.1-c). Next, a salicidation process is applied to form about 30-nm-thick NiSi film on the junction (Fig.1-d). Because the n+ region extends about 500nm outside the sidewalls and the NiSi formation is well contained within the n+ region, these junctions allow extraction of an innate perimeter leakage similar to the one expected at a gate edge (i.e. the leakage induced purely by the presence of the NiSi film edge). Furthermore, absence of heavy implantation damage enables these junctions to illuminate intrinsic properties of the NiSi film.

3. Leakage Generation; Si(110) vs. Si(100)

In order to assess the impact of thermal processing on junction leakage, the above junctions were post-annealed in N_2 at 400^{o}C, 450^{o}C and 500^{o}C for up to 90min. In Fig.2 and Fig.3, areal leakage levels of Si(110) and Si(100) substrates are respectively plotted as functions of the junction depth for each post-anneal condition (right axes) and correlated with Ni backside SIMS profiles (left axes). The excellent matching between the leakage-depth profiles and Ni SIMS data provides direct evidence of Ni involvement in the GR center formation as a root cause of the leakage in both substrates. Moreover, irrespective of the substrate orientation, the matching is obtained with the same proportionality (i.e., correspondence between left and right axes), suggesting similar effective cross-section of Ni of about 2.0×10^{-14} cm^2 (i.e., much larger than that of atomic Ni [4]). This consistent agreement indicates an identical physical origin of the leak-generating Ni defects (i.e., Ni clusters [3]) regardless of the substrate orientation. In fact, in all cases, temporal evolutions of the leakage depths (at $I_R=10^{-7}$A/cm^2) are describable with fast initial ingression (by burst of small precursors of Ni clusters from NiSi) and subsequent slower diffusion (by rapid coalescence into larger clusters) (Fig.4), as formulated in ref. [3]. Kinematic similarity of 400^{o}C and 450^{o}C data further corroborates the substrate-independence of these rather benign low temperature defects. Strikingly, however, at 500^{o}C, leakage and SIMS profiles in Si(110) substrates remain virtually immobile throughout the annealing, whereas a sizeable inward migration is clearly visible for Si(100). Yet a shared origin of these defects is still supported by the convergence of the activation energies as a function of leakage level (Fig.5). Immobility in Si(110) substrate of otherwise movable Ni clusters at 500^{o}C (as is the case for Si(100)) means restriction of Ni migration within a plane parallel to the substrate surface(i.e., (110)). Note that the strong anisotropy even singles out the (110) plane among other symmetrically equivalent {110} planes. As illustrated in Fig.6, this proves the presence of Ni cluster's own specific directional structure incompatible with the crystal symmetry of Si and also implies preferential formation of directional defects depending on the surface orientation from which Ni is released. In order to gain an additional insight into the anisotropy, Fig.7 and Fig.8 plot perimeter leakage components corresponding to Fig.2 and Fig.3. Putting aside a good correlation in general, conspicuously, at 500^{o}C, a small but unmistakable ingressive movement is in evidence at the periphery of the Si(110) junctions (Fig.7) unlike the areal data (Fig.2). Despite this temporal disparity, congruent shapes of I-V curves (Fig.9) nonetheless validates the common origin of the leakage between areal and perimeter components. In view of the extension of junctions beyond the NiSi films, the Ni induced perimeter leakage is obviously generated inside the Si substrate below the NiSi edges, not at any isolation interfaces. Indeed, by appropriately defining the perimeter leakage depth (at $I_R = 4\times10^{-10}$A/cm), the temporal evolution of 500^{o}C data at the Si(100) perimeter can be decomposed into burst and diffusion almost identical to those for the areal data (Fig 10), implicating the same mechanism behind the perimeter leakage. The distinguishing compounded kinematics also holds at the Si(110) perimeter, but with a notably slower diffusivity. At the bottom of NiSi on (110), Ni cluster's deeper ingression was inhibited by its exclusive formation on (110) (Fig.6). Then, as depicted in Fig.11, the distinct downward mobility observed at the Si(110) perimeter signifies Ni cluster formation on some {110} planes other than (110), possibly due to a geometrically incoherent burst at the NiSi edges. Furthermore, the discrepant diffusivities along <100> and <110> point to yet another directional preference of Ni cluster's migration even within the {110} planes. With all {110} carefully considered, the diffusion ellipsoid [5] of the Ni cluster at 500^{o}C, which is already shown to be degenerated within one of {110} planes, is now found to be about 1.7 times elongated toward <100> (Fig.12).

4. Summary and Conclusion

Thermally induced leakage from NiSi on Si(110) is thoroughly investigated and evidence of anisotropic Ni migration is secured. Similar to NiSi on Si(100), thermal instability could pose a serious threat to shallow junctions on Si(110) substrate with NiSi, especially at junction edges. Although the leakage is alleviated by anisotropic Ni migration compared to Si(100) substrate, means to stabilize NiSi films against heat stimulus is better to be developed.

References

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[2] C.Y.Sung et al, *IEDM Tech. Dig*., 2005 , p.235
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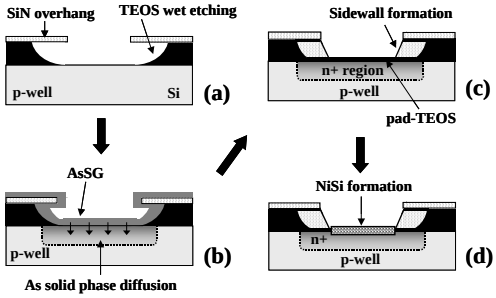

Fig.1 n+/p junction formation procedure to fabricate damage-free diodes. Solid phase diffusion from AsSG is used for creating n+ region. NiSi formation is well contained within the n+ region.

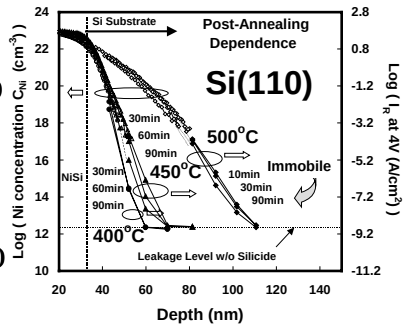

Fig.2 Comparison between Ni SIMS profiles and leakage-depth profiles of Si(110) substrates after 400°C, 450°C and 500°C annealing for up to 90min.

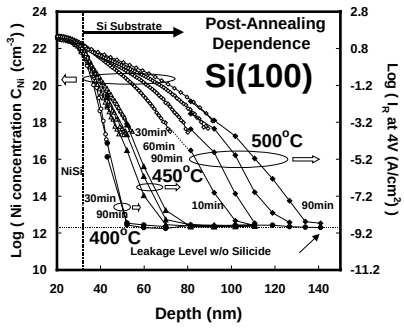

Fig.3 Comparison between Ni SIMS profiles and leakage-depth profiles of Si(100) substrates after 400°C, 450°C and 500°C annealing for up to 90min.

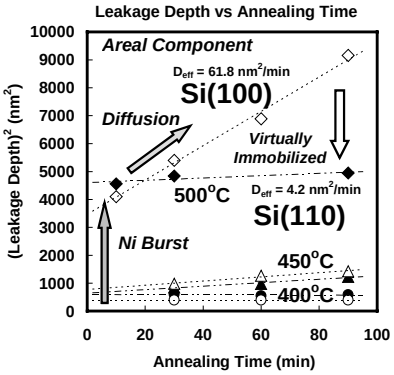

Fig.4 Ni migration kinematics represented as temporal evolution of square of leakage depth during annealing for both Si(110) and Si(100) substrates. Burst and diffusion are basic components of the migration

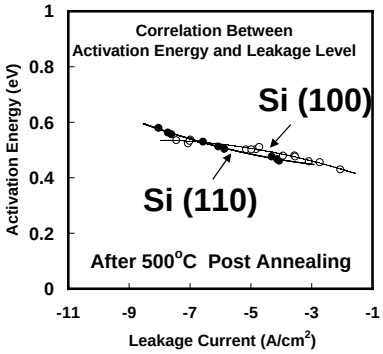

Fig.5 Activation energies of the leakage current plotted as a function of leakage level. Similarity of the activation energy shows identical origin of leakage regardless of the substrates

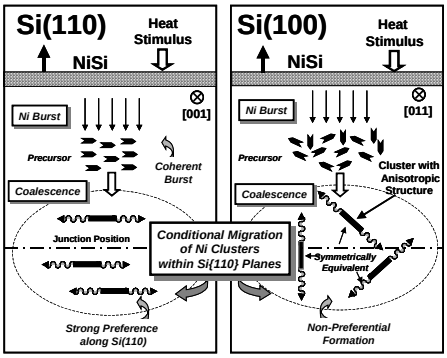

Fig.6 A model explaining asymmetric leakage generation between Si(110) and Si(100) substrates. Along [110], aligned burst of small Ni clusters promotes formation of large directional defects movable only within Si(110) plane.The same defects produced in Si(100) substrate can migrate along several equivalent Si{110} planes.

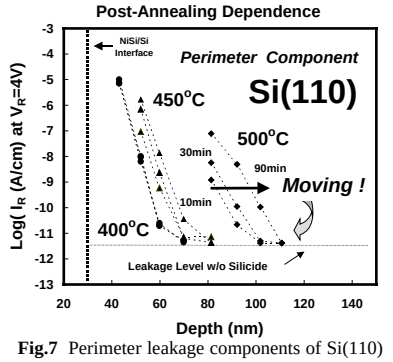

Fig.7 Perimeter leakage components of Si(110) substrates plotted as functions of junction depth for annealing conditions corresponding to Fig.2

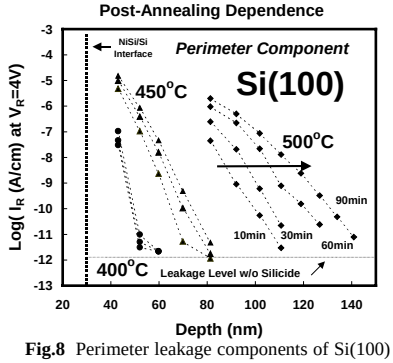

Fig.8 Perimeter leakage components of Si(100) substrates plotted as functions of junction depth for annealing conditions corresponding to Fig.3

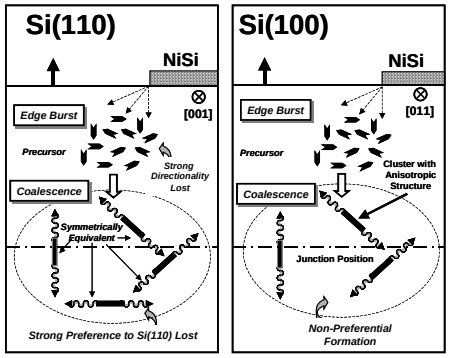

Fig.11 A model explaining perimeter leakage in Si(110) and Si(100) substrates. At NiSi edge on Si(110), directional defects are allowed to migrate along several equivalent Si{110} planes other than (110). The leakage mechanism at NiSi edge on Si(100) is identical to NiSi bottom

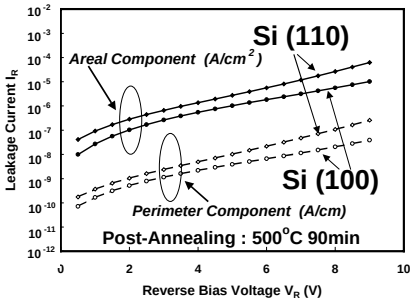

Fig.9 Reverse bias dependencies of areal and perimeter leakage components for both Si(100) and Si(110) substrates after 500°C, 90min post-annealing. Junction depths are 119nm and 92nm for Si(100) and Si(110), respectively.

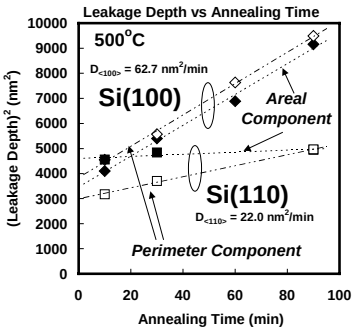

Fig.10 Ni migration kinematics represented as temporal evolution of square of leakage depth of areal and perimeter components during 500°C annealing for both Si(110) and Si(100) substrates.

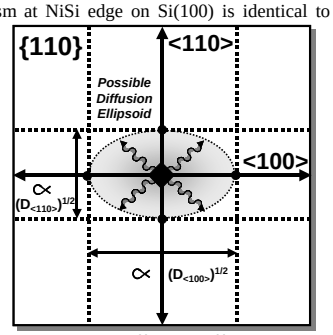

Fig.12 Anisotropic effective diffusion ellipsoid of Ni clusters at 500°C in the Si substrate along {110}, stretched about 1.7 times toward <100>.