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Reduction in PN Junction Leakage for Ni-silicided Small Si Islands by Using Thermal Conduction Heating with Stacked Hot Plates

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Abstract

In conventional self-aligned Nickel (Ni) silicide (SALICIDE) process, Ni silicidation is carried out by using tungsten-halogen lamp annealing and pn junction leakage current increases with the miniaturization of junction area. It was found that the junction leakage is closely related to Ni silicide thickness which is determined by absorption coefficient of infrared light from the halogen lamp. The pattern dependence of junction leakage and Ni silicide thickness of small source and drain (S/D) islands has not been sufficiently investigated so far. In this paper, we proposed a new method for Ni silicidation based on conductive heat transfer to the wafer and confirmed that this method can drastically improve the pattern dependence of pn junction leakage due to better uniformity of Ni silicide thickness independent of pattern size of active areas.

Introduction

Ni monosilicide (NiSi) has an advantage of less silicon consumption as compared with $CoSi_2$ and can be formed at lower temperature (<500 °C)[1]. Therefore, NiSi is eminently suitable for shallowing the pn junction depth of MOSFETs. In conventional Ni SALICIDE process, Ni silicidation is carried out by using tungsten-halogen lamp annealing. However, there is a serious issue that junction leakage current for small S/D island areas is higher than at the wider area. The increase in junction leakage in small islands was caused by the thicker Ni silicidation at the edge of small islands[2]. Reducing the thermal budget of the silicidation anneal step was found to avoid the thicker Ni silicidation at the edge of small islands and improve the junction leakage in small islands[3]. However, as the junction depths become shallower, reducing the thermal budget of the silicidation anneal step can not reduce the junction leakage. In addition, the pattern dependence of junction leakage and Ni silicide thickness of Ni-silicided small islands have not been sufficiently investigated so far.

In this paper, we studied the pattern dependence of junction leakage of Ni silicided small islands and we newly found the isolation width dependence of junction leakage. In order to improve the pattern dependence of junction leakage for small islands, we applied a new method for silicidation by using stacked hot-plates which utilize conductive heat transfer to the wafer. This method drastically reduces the thickening of Ni silicide at the edge of small islands and successfully improved the junction leakage of small islands.

Experimental

A fundamental process flow of Ni SALICIDE formation is shown in Fig. 1. Ni films were sputtered on silicon wafers with various patterns of STI (SiO_2). Ni silicidation was carried out as follows. A silicon wafer is placed on a hot-plate and another hot-plate is set proximity of the front surface of the wafer. The hot-plate annealing was performed for 300 s in nitrogen ambient. For comparison, the conventional rapid thermal process (RTP), that is tungsten-halogen lamp annealing, was performed for 30 - 90 s at temperature below 300 °C in N_2. After unreacted Ni films were selectively removed by wet etching and the whole of Ni silicide was converted to NiSi during second step RTP in N_2. Measured diode pattern consists of 17.000 active area islands. The island size is 0.3 μm. The width of the isolation is varied from 0.13 to 0.8 μm. The excessive Ni silicide thickness was investigated by using cross-sectional transmission electron microscopy (XTEM). The junction leakage was measured at a reverse bias of 2 V.

Results and Discussion

In the case of conventional tungsten-halogen lamp annealing which is based on radiative heat transfer to the wafer, the junction leakage current for small silicon island area was higher than that at the wider silicon island area. In reference [3], the increase in junction leakage for small islands was reported to be caused by the thicker Ni silicide formation at the edge of small island area, because a continuous supply of Ni from an extra Ni on top of the isolation surrounding island silicon areas. However, it was found that the leakage current for 0.3 μm island increases with narrowing isolation width as shown in Fig. 2. It is considered that the thicker Ni silicide formation can be suppressed if the isolation width becomes narrow, since total volume of excess Ni on the isolation region becomes less in the case of narrow isolation width. Therefore, we considered the cause of the difference in NiSi thickness

is the difference in the surface temperature of the wafer, we simulated the relationship between absorbed power and the isolation width in small island in tungsten-halogen lamp annealing as shown in Fig. 3. Simulation results showed that absorbed power at the narrowest isolation width was higher than at the wider isolation width. And more specifically, it was indicated that the narrower isolation patterns reached higher temperature than the wider isolation patterns in the case of using lamp annealing. That is, it is considered that increase in Ni silicide thickness and junction leakage in small island and the narrowest isolation patterns were caused by pattern-induced localized heating effects in the case of lamp annealing, as illustrated in Fig. 4. To achieve the homogeneous Ni-silicidation independent of the pattern size effects, it is necessary to apply a new method for the Ni-silicidation based on conductive heat transfer to the wafer. Therefore, we investigated the hot-plate based annealing for first step Ni-silicidation annealing. Table 1 shows a comparison between conventional lamp annealing and the hot-plate annealing. In the hot-plate annealing, the wafer temperature initially increases gradually and then it saturates at little below the hot-plate temperature. The heat transfer between the hot-plates and the wafer is predominated by thermal conduction through an ambient gas. At first, from XTEM analysis, the hot-plate annealing was found to suppress the thickening of Ni silicide in small silicon islands. It was clarified that the hot-plate annealing effectively suppress the thickening of Ni silicide at the edges of small island areas as compared with halogen lamp annealing as shown in Fig. 5 (a) and (b), XTEM image of 0.3 μm island and the ratio of Ni silicide thickness at the edge of island to that at the center of island for hot-plate annealing and lamp annealing. Then, we studied the effect of hot-plate annealing on electrical properties of Ni silicide. Fig. 6 shows the normalized sheet resistance of Ni silicide active area lines as function of line width for hot-plate annealing and lamp annealing. By using hot-plate annealing, it was found that the thickening of Ni silicide at the edges of active areas was effectively suppressed and as a result, reverse narrow line effect of sheet resistance was successfully improved as shown in Fig. 6. Fig. 7 (a) and (b) show cumulative probability plots of junction leakage measured for 0.3 μm island with 0.13 μm isolation width and 0.8 μm isolation width for n+/p junction comparing hot-plate annealing and lamp annealing. Hot plate silicidation drastically improves the junction leakage current distribution especially for narrower isolation width. Furthermore, the isolation width dependence of measured junction leakage current in 0.3 μm island was remarkably improved as shown in Fig. 8.

Conclusions

It was clarified that the junction leakage current for small island at the narrowest isolation width is higher than at the wider width and the junction leakage is closely related to Ni silicide thickness which is determined by absorption coefficient of infrared light from the halogen lamp in the case of using lamp annealing. Hot-plate annealing based on conductive heat transfer to the wafer was found to significantly improve the pattern dependence of junction leakage and thicker silicidation of small Ni-silicided S/D islands. The pattern dependence of junction leakage and thicker silicidation in small island active area is due to the homogeneous Ni silicidaiton independent of the pattern size. It has been shown that the hot-plate based annealing can realize the formation of Ni silicide for ultra-shallow junctions for high-performance devices.

Acknowledgements

References

[1]   T. Morimoto et al., IEEE Trans. Electron Dev. **42** (1995) 915-922.
[2]   F. Deng, et al., J. Appl. Phys. **81** (1997) 8047-8051.
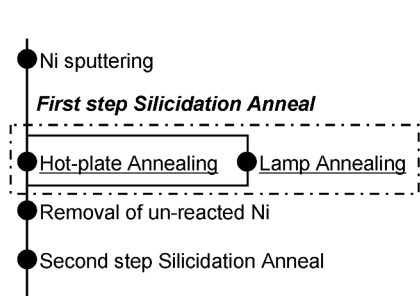[3]   A. Lauwers, et al., Microelectron. Eng., **76**, (2004) 303-310.

Fig.1 Process flow diagram of Ni SALICIDE formation.

- Ni sputtering

First step Silicidation Anneal

Hot-plate Annealing — Lamp Annealing

- Removal of un-reacted Ni
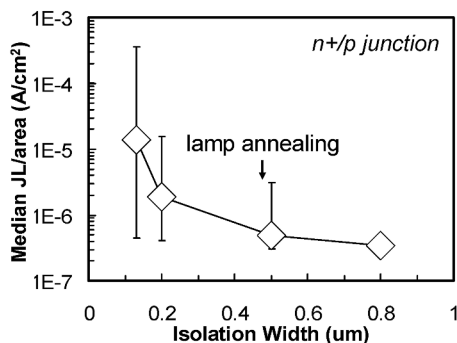- Second step Silicidation Anneal

Fig.2 Junction leakage measured at 2 V reverse bias on 0.3 μm island patterns as function of isolation width (n+/p junction, lamp annealing for 90 s at 275 ˚C).
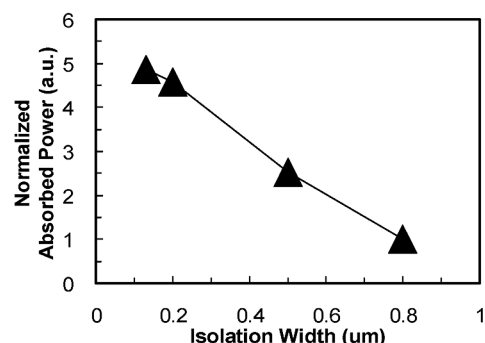

Fig.3 Simulated relationship between normalized absorbed power and the isolation width on 0.3 μm island pattern in tungsten-halogen lamp annealing.
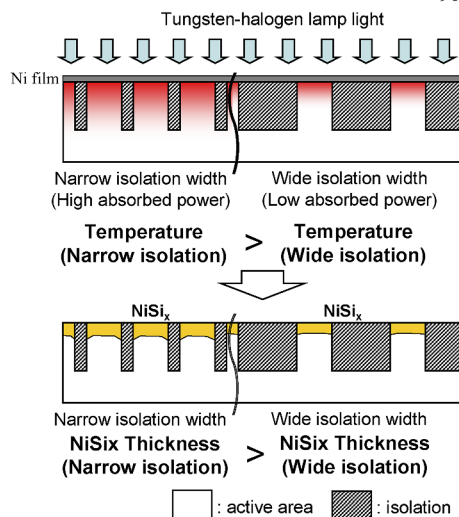

Fig.4 Schematic diagram of pattern-induced localized heating effects in the case of lamp annealing.

Tungsten-halogen lamp light

Ni film

Narrow isolation width (High absorbed power) | Wide isolation width (Low absorbed power)

Temperature (Narrow isolation) > Temperature (Wide isolation)

NiSi$_x$ | NiSi$_x$

Narrow isolation width | Wide isolation width

NiSix Thickness (Narrow isolation) > NiSix Thickness (Wide isolation)

□ : active area   ▨ : isolation

Table 1. Comparison between conventional halogen lamp annealing and hot-plate annealing.

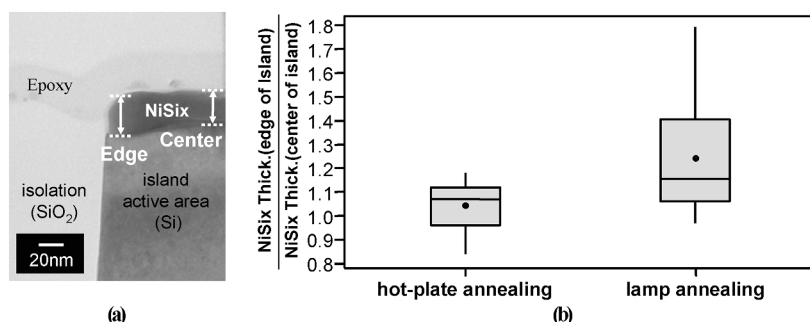|	Lamp Annealing	Hot-plate Annealing
Heat transfer	Radiation	Conduction
Pattern effect	NG	OK
Emissivity effect	NG	OK

Fig.5 (a) XTEM image of 0.3 μm island. (b) Boxplots of the ratio of Ni-silicide thickness at the edge of island to that at the center of island.
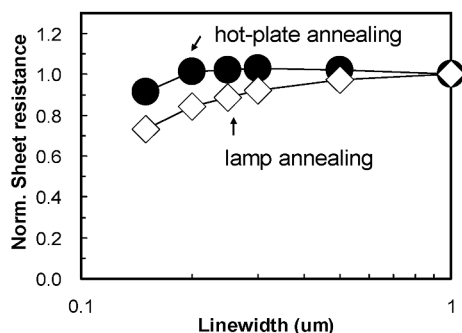
Epoxy — NiSix — Center — Edge — isolation (SiO$_2$) — island active area (Si) — 20nm

NiSix Thick.(edge of Island) / NiSix Thick.(center of island)

hot-plate annealing | lamp annealing

(a)   (b)

Fig.6 Normalized sheet resistance of Ni silicide active area lines as a function of line width for hot-plate annealing and lamp annealing.
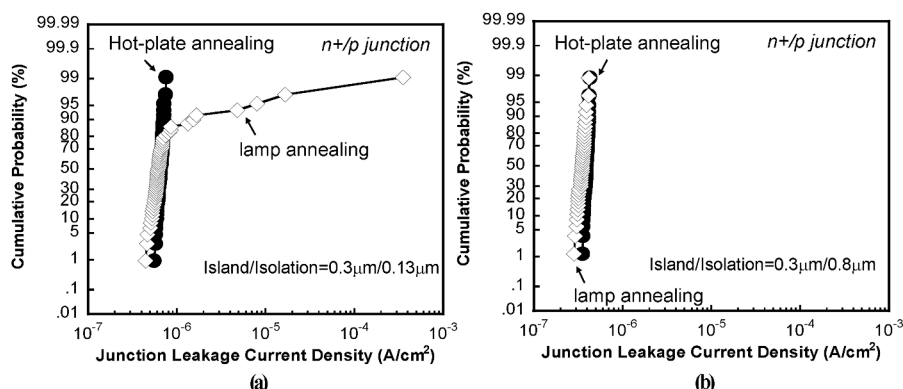

Fig.7 Cumulative probability plot of junction leakage measured at 2 V reverse bias on 0.3 μm island patterns for hot-plate annealing and lamp annealing (n+/p junction). (a) 0.13μm isolation width. (b) 0.8μm isolation width.
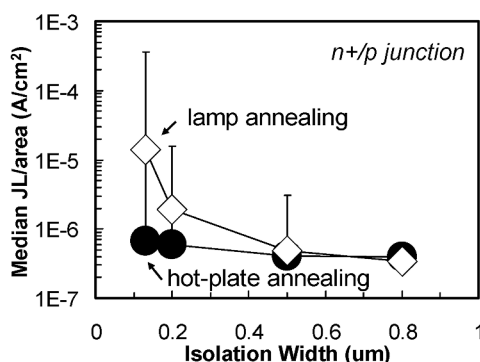
(a) Island/Isolation=0.3μm/0.13μm

(b) Island/Isolation=0.3μm/0.8μm

Fig.8 Junction leakage measured at 2 V reverse bias on 0.3 μm island patterns as function of isolation width for hot-plate annealing and lamp annealing (n+/p junction).