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E-6-2

A Novel Laser Annealing Process for Advanced CMOS with Suppressed Gate Depletion and Ultra-shallow Junctions

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1. Introduction

The gate depletion of poly-Si gate electrode and off current increase caused by gate leakage can not be ignored in advanced CMOS devices due to aggressive scaling in gate oxide thickness. Although high-k gate dielectrics and metal gate electrodes are intensively studied, strong demand for dual ploy-Si gate/ nitrided gate oxide technology still exists for SoC device fabrication. Formation of highly doped and ultra-shallow junctions at source and drain (S/D) is another big challenge in advanced CMOS. For this purpose spike rapid thermal annealing (RTA) has been mainly employed but further reduction of thermal budget is required. Although laser spike annealing (LSA) is promising for ultra-shallow S/D formation [1], it makes the gate depletion severer since the dopants in the gate are usually activated using the same annealing step that forms the S/D regions for process simplicity and thus the dopants can not diffuse to the gate/gate oxide interface. We propose a gate pre-annealing by laser thermal process (LTP) in conjunction with LSA for S/D activation to solve these problems. The effects on the gate depletion, dopant penetration and transistor performance are discussed.

2. Experimental

We fabricated CMOS devices using a process flow shown in Fig. 1. Laser thermal melting process using XeCl excimer laser (λ=308nm) was used to activate dopants in gate electrode. In order to melt amorphous Si (α-Si) layer for gate electrodes without melting the crystalline Si underlying the gate oxide (Si-sub), thickness of 1st α-Si layer was set to be 60nm. We also investigated the device performance in relation to S/D activation annealing.

3. Results and discussions

Secondary ion mass spectometry (SIMS) profiles of B and O concentration in poly-Si gate are shown in Fig. 2. The thermal budget of LSA is insufficient to diffuse B atoms to gate/gate oxide interface, resulting in B concentration less than $3\times10^{19}cm^{-3}$. In LTP devices, the selective melting and re-crystallization transformed doped α-Si to poly-Si and made the dopant concentration at the poly-Si gate/gate oxide interface to be $2\text{-}5\times10^{20}cm^{-3}$. The CV characteristics of PMOS fabricated by LTP and various S/D activation annealing are compared in Figs. 3 and 4. Spike RTA devices caused a slight positive shift in flat-band voltage (Vfb). SIMS results indicate that the Vfb shifts are due to B penetration. Large O_2 mixing in SIMS profile of spike RTA devices also suggests the severe B penetration. A high dose of B implantation for pre-doping the gate electrode also tends to induce B penetration. By using LSA for S/D activation, Vfb shift can be suppressed; however gate depletion becomes large. These imply that there is a trade-off between suppression of gate depletion and B penetration. LTP+spike RTA gives thinnest electrical inversion oxide thickness (T_{inv}) but causes Vfb shift in PMOS. At Vg=1.0 V, the LTP (800mJ)+LSA device shows no Vfb shift and about 0.10nm improvement of gate depletion leading to smaller T_{inv} both in NMOS and PMOS compared to the spike RTA device with gate annealing (Fig. 5), resulting in I_{ds} increase (Fig. 6(a)). ΔVth in PMOS is about 100mV which well coincides with the result of Vfb shift in CV characteristics (Fig. 6(b)). TEM micrographs of poly-Si gate electrodes in the RTA and LTP devices after complete CMOS fabrication are shown in Fig. 7. The final grain structure of the LTP device shows relatively uniform distributions of nm-grains because LTP transforms α-Si into poly-Si with smaller size of grains. In the RTA device, in contrast, grains are large and have pillar-like structure due to random nucleation during crystallization. Another favorable effect of the LTP device is smaller off current (I_{off}), which is due to the reduction of gate leak current as shown in Fig. 6(b). This is attributable to the nm-grains of poly-Si, which can decrease the concentration of segregated dopants at gate/gate oxide interface and suppress a local electric field enhancement [2, 3] (Fig. 8).

In LTP devices, no mobility degradation by melt and re-crystallization process at higher temperature can be seen and the mobility behaviors of the LSA and spike RTA are almost identical, which indicates the high temperature LTP and LSA does not affect the gate oxide interface quality (Fig. 9). Even with highly activated gate, no degradation of hot carrier lifetime in NMOS occurred. In PMOS, severe NBTI degradation caused by B penetration was observed for spike RTA devices as shown in Fig. 10. From this result, we suggest that gate activation by LTP should be followed by sub-millisecond annealing of LSA for S/D activation.

4. Conclusions

We have successfully demonstrated a novel process module using LTP and LSA that can effectively suppress poly-Si gate depletion while achieving highly activated ultra-shallow junctions in S/D, leading to improved transistor performance. Moreover, I_{off} was reduced more than one order of magnitude compared with conventional spike RTA devices.

References

[1] A.Shima, et. al. Symp. on VLSI Tech., p174 (2004)
[2] M.Ushiyama, et. al. Tech. Dig. IRPS pp 3331 (1991)
[3] S. Muramatsu, et. al. Tech. Dig IEDM pp 847 (1994)

Shallow Trench Isolation
Well & Vth Adjust Implants
Gate Oxide Formation with nitridation
(Topt.1.5nm)
α-Si depo 60nm + Gate Implantation
LTP melt (XeCl 308nm 400-800mJ/cm²)
or w/o annealing
α-Si depo 70nm + Gate Imp.
Gate Patterning
Source/Drain Extensions Imp.
Low temperature Spacer
Deep Source/Drain I.I.
SD annealing
1050°C spike RTA
LSA 1300°C 800μs
RTA 800°C 10s
Salicidation & Metallization

Ref.
polySi 130nm+ Gate Imp.
+RTA pre-annealing
+1050°C spike RTA
(SD annealing)

Fig. 1 CMOS fabrication process flow in this work

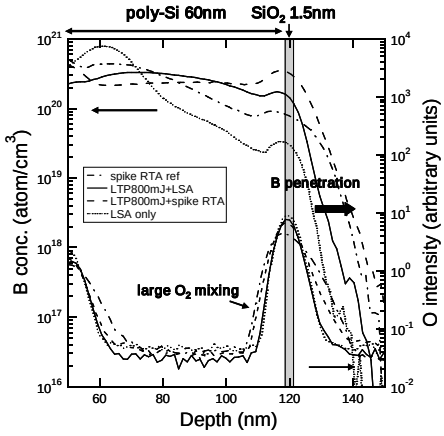

Fig. 2. SIMS profiles of B and O concentration in poly-Si gate by various annealing

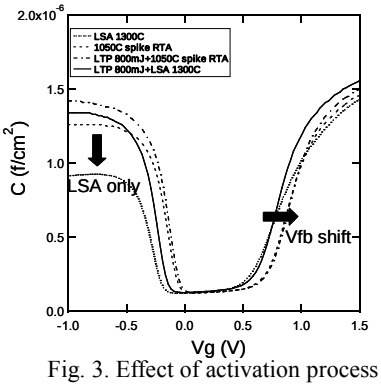

Fig. 3. Effect of activation process in this study on T_{inv} improvement and Vfb shift

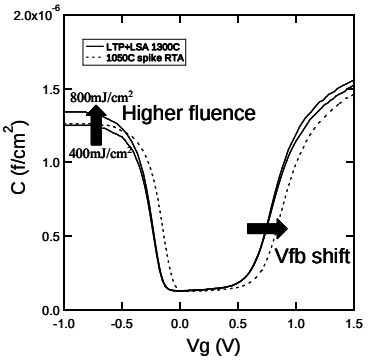

Fig. 4. Effect of laser fluence of LTP on T_{inv} improvement and Vfb shift by spike RTA

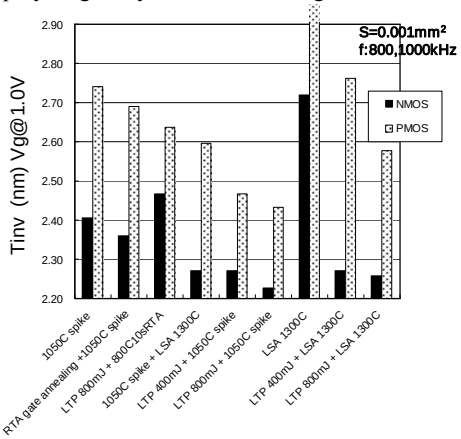

Fig. 5 Comparison of T_{inv} among various re-crystallization and S/D activation annealing

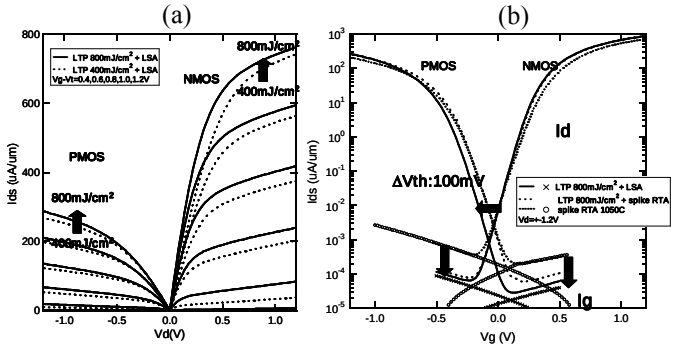

Fig. 6 (a) Id-Vd and (b) Sub-threshold Id-Vg characteristics of CMOS devices Lg:0.2μm

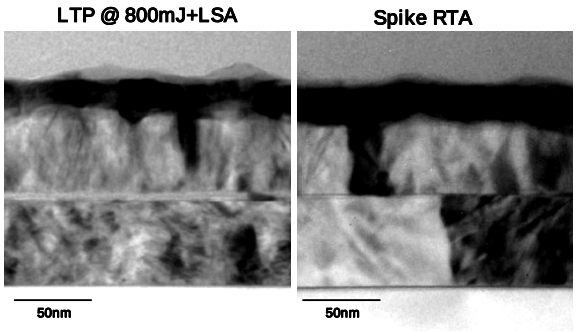

Fig. 7 Cross-sectional TEM image of poly-Si layer formed by LTP+LSA and spike RTA

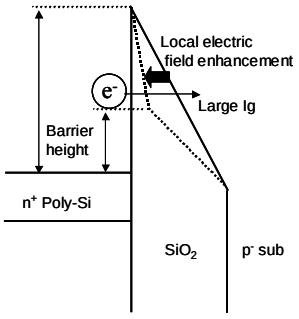

Fig. 8 Schematic illustration of local electric field enhancement by dopant segregation at gate/gate oxide interface

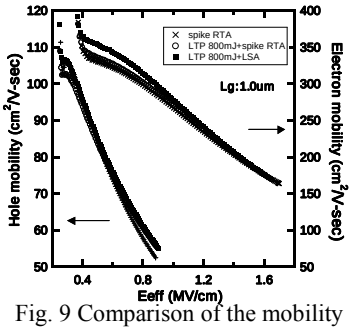

Fig. 9 Comparison of the mobility in CMOS between LTP and spike RTA for gate recrystallization and between spike RTA and LSA for S/D activation

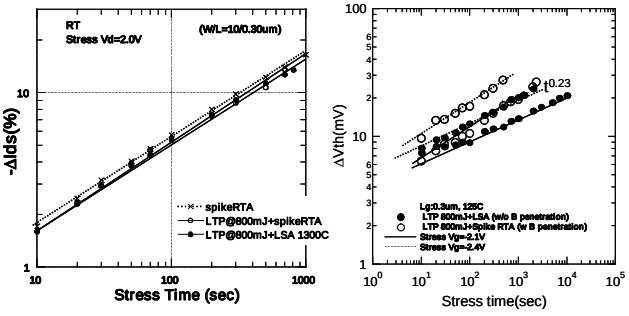

Fig. 10 Hot carrier lifetime of NMOS and Negative Bias Temperature Instability of PMOS fabricated by LTP for gate activation and spike RTA or LSA for S/D activation