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Enhancement Mode GaAs n-MOSFET with High-k Dielectric

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1. Introduction

Fermi level pinning at the semiconductor-gate oxide interface is a major challenge for III-V based MOSFETs[1] calling for effective surface passivation. The role of a Si layer in passivation of the surface states at the GaAs interface has been intensively studied[2,3]. We have recently demonstrated effectiveness of a Si interface layer for *in situ* passivation of MBE grown GaAs surface enabling good electrical characteristics of MOS capacitors with HfO_2 gate dielectric[4]. In this work, we demonstrate performance of enhancement mode N-MOS transistors fabricated on MBE grown GaAs with an in-situ Si passivation layer, ex-situ deposited HfO_2 gate dielectric and TaN metal gate.

2. Experimental

The samples for n-MOSFETs were grown by molecular Beam Epitaxy (MBE) in an EPI GEN II system on a semi-insulating GaAs substrate. A 70-nm thick un-doped GaAs channel was separated from the wafer bulk by a 100 nm thick $Al_{0.3}Ga_{0.7}As$ barrier and a thin p-type $Al_{0.3}Ga_{0.7}As$ layer doped with carbon to 2×10^{17} cm^{-3} to compensate possible background doping of the GaAs channel. This modulation doping resulted in a sheet holes concentration of 7×10^{11} cm^{-2}. Simulated band diagram of the MOSFET at a positive gate bias is shown in Fig. 1.

A capping layer of 1.5 nm thick amorphous Silicon was deposited in-situ to passivate the GaAs surface immediately after the growth. Deposition was performed onto a cold (~60 ^{0}C) substrate using Si effusion cell. The gate stack, consisting of 10 nm HfO_2 and ~0.2 μm TaN was ex-situ deposited using Physical Vapor Deposition method[5] within two days after MBE growth. Transistors with a ring-shape geometry were processed using self-aligned Si ion implantation into the source and drain regions and the open GaAs gap areas to a dose of 10^{14} cm^{-2}. Implanted spices were activated by rapid thermal annealing at 700 ^{0}C for 10 sec. Although this post-implantation anneal was expected to activate only a few percent[6] of implanted impurities and thus result in significant series resistance, the low annealing temperature was chosen not to compromise the properties of the gate stack. The Au-Ge based Ohmic contacts were deposited onto the source and drain regions using a separate mask with 20 μm gaps between contacts and the gate. To minimize the effect of S/D contact resistance we measured large ring-shape transistors with L/W ~ 0.14.

3. Results and discussion

A TEM cross-section of the gate stack is presented in Fig. 2. Interface between mostly oxidized Si passivation layer and GaAs remains atomically sharp after annealing up to 800 ^{0}C, though at temperatures 750 ^{0}C and above we found an increase of the gate leakage current.

The I_d-V_g characteristics demonstrating V_T of 0.09V and high transconductance $G_{m\ max}$ = 88 mS/mm are shown in Fig. 3. The threshold gate voltage indicates an enhancement mode operation of the fabricated transistors. The I_d-V_d characteristics with $g_{d\ max}$ = 0.65 mS shown in Fig. 4 correspond to operation of MOSFET with n-channel. The maximum channel sheet carrier concentration is evaluated to be as high as 6×10^{12} cm^{-2} cm^{-3} strongly indicating formation of an inversion channel. Indeed, the background electron concentration in an undoped GaAs channel can not be responsible for the channel conductance. To provide such sheet carrier concentration the GaAs layer must have contained up to 10^{18} electron/cm^3 and a large negative V_g would be needed to deplete the channel. This consideration strongly confirms an enhancement mode operation of an n-MOS transistor. The channel to gate C-V characteristics with oxide capacitance of 0.8 μF/cm^2 is shown in Fig. 5. Effective electron mobility is calculated from measured electron concentration and drain current, and is shown if Fig. 6. The maximum channel electron mobility is estimated as 300 cm^2/V·s. To increase the channel mobility we need to improve the GaAs interface quality and reduce density of electron traps in high-k dielectric.

4. Summary

GaAs enhanced mode transistor with n-channel is demonstrated using HfO_2 high-k dielectric. *In situ* deposited Silicon surface passivation layer was used to prevent pinning of Fermi level at the surface of device. Threshold voltage of 0.06 V proves enhanced mode operation of FET. Maximum measured transconductance of 88 mS/mm is limited by series resistance of contacts and wide gaps between the contacts and gate of the device.

References

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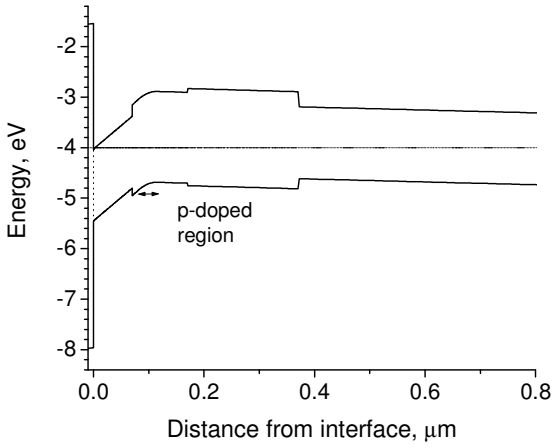

Figure 1 Band diagram of GaAs MOSFET in ON state (positive voltage applied to gate)

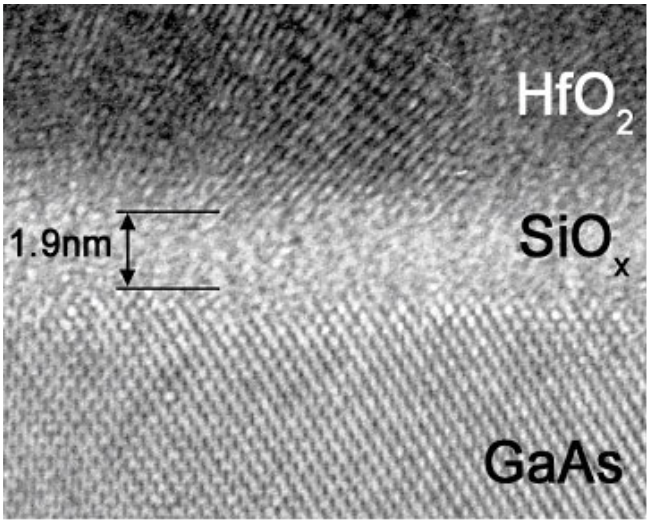

Figure 2 High resolution cross-sectional TEM of GaAs/SiO_x/HfO2 interface.

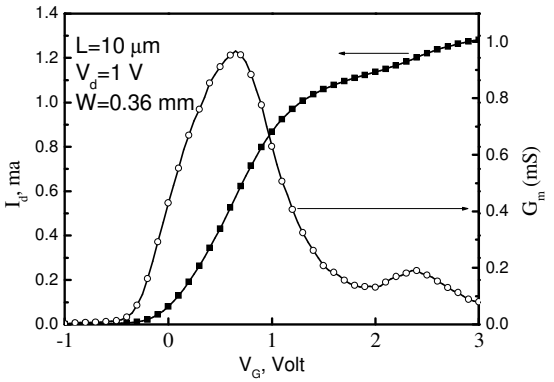

Figure 3. I_d-V_g and g_m-V_g characteristics of GaAs MOSFET with L/W=0.14.

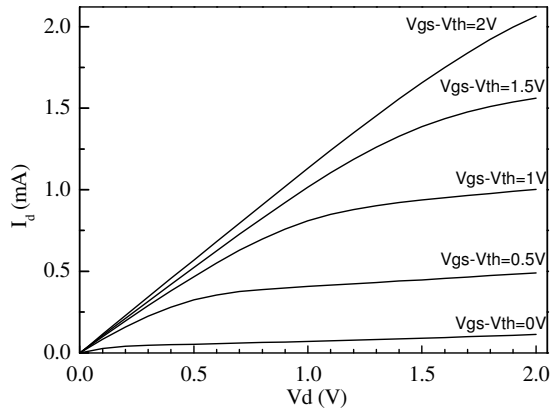

Figure 4. I_d-V_d characteristics of GaAs MOSFET with L/W=0.14.

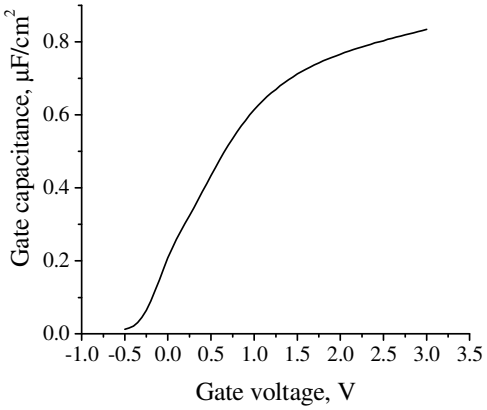

Figure 5. Gate-to-channel C-V characteristics of GaAs MOSFET

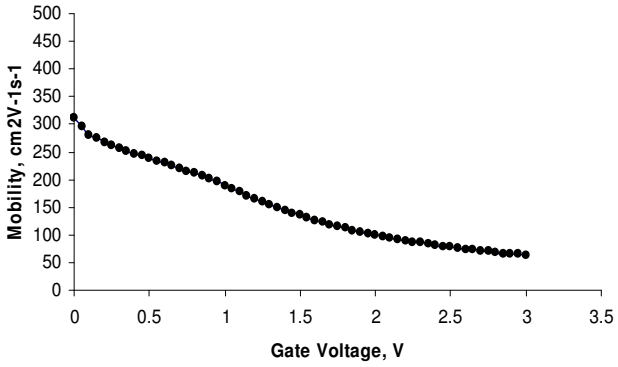

Figure 6. Effective electron mobility as a function of gate voltage on GaAs MOSFET