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80nm T-Shaped Gate Metamorphic HEMTs fabricated Using Two-Step Gate Recess Process

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1. Introduction

InAlAs/InGaAs high electron mobility transistors (HEMTs) on InP substrates have shown the high frequency characteristics, low noise figure, high gain and efficiency [1~2]. However, the cost, size, and fragility of the InP wafers are an obstacle to commercial applications of InP HEMT devices. Metamorphic high electron mobility transistors (MHEMTs) on GaAs substrate are increasingly becoming important for the fabrication of millimeter-wave MMICs with high power and low noise applications [3~4]. For MHEMTs, the gate recess processing is critical to achieve both performance and uniformity of the devices. Selective gate recess is widely used to etch the InGaAs layer over InAlAs, which causes to control poor recess width [5]. Therefore, the precise etch depth and recess width control are required for gate recess process.

In this paper, we report the DC and microwave performance of 80nm T-shaped gate length $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ low noise MHEMT on GaAs substrate fabricated using two-step gate recess process, which results from the precise etch depth and reduced recess width.

2. Fabrication Process

The low noise MHEMT epitaxial structure on GaAs substrate has been grown by molecular beam epitaxy (MBE). The cross-section of low noise MHEMT structure is shown in Fig. 1.

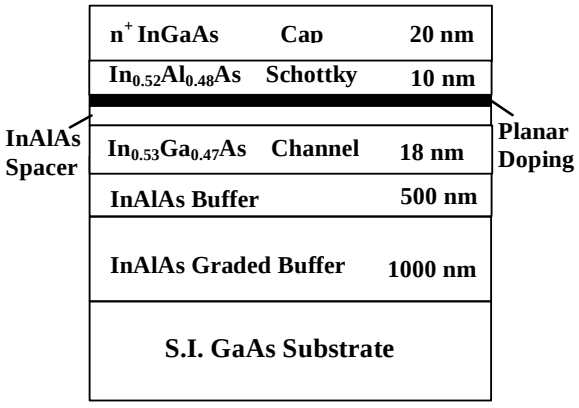

Fig. 1. Cross-section of low noise MHEMT structure.

A 1 μm thick In-graded InAlAs metamorphic buffer layer was grown on a 4-inch diameter semi-insulating GaAs wafer, followed by a 500 nm thick undoped InAlAs buffer layer. We used 18 nm $In_{0.53}Ga_{0.47}As$ as the channel layer. The Si-planar doping layer was separated from the channel layer by 3 nm thin undoped $In_{0.52}Al_{0.48}As$ spacer. The undoped $In_{0.52}Al_{0.48}As$ Schottky layer was 10 nm. Then, the 20 nm thick $In_{0.53}Ga_{0.47}As$ cap layer was highly doped with Si of 5×10^{18} cm^{-3}. Hall measurements of MHEMT structure yielded an electron sheet density of $n_s = 3.2 \times 10^{12}$ cm^{-2} and mobility of μ_H = 9,100 $cm^2/V \cdot s$ at 300K.

MHEMT devices with T-shaped gate of 80nm gate length and 100 μm gate width were fabricated. The ohmic drain-to-source distance of 2 μm was used. The sequence for device fabrication is as follows. After mesa isolation by H_3PO_4 based-wet chemical etching, AuGe/Ni/Au metallic layers were deposited as the ohmic contacts. For 80nm T-gate process, bi-layer resists which consist of P(MMA-MAA)/PMMA were exposed using 100kV electron beam lithography system. Then, the two-step gate recess was performed using the succinic acid- and citric acid-based etchant to obtain both precise etch depth and recess width on the devices. Ti/Pt/Au (0.5 μm thick) metals were used for the T-gate metallization. After the formation of T-gate electrode, SiN layer of 50nm was deposited by plasma-enhanced chemical vapor deposition (PECVD) to passivate the devices. Fig. 2 shows a cross-sectional SEM of 80nm T-gate MHEMT obtained with two-step gate recess. It shows that a reduced recess width of 50nm was achieved on the each side of gate.

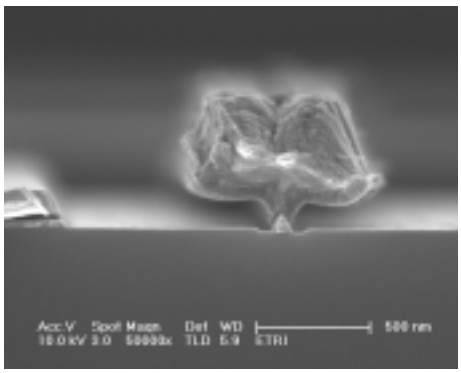

Fig. 2. Cross-sectional SEM of 80nm T-gate MHEMT with recess width of 50nm.

3. Results

The 80nm gate-length low noise MHEMTs with T-gate were characterized for DC and microwave performance. Fig. 3 shows drain current as a function of source-to-drain voltage (V_{ds}) for MHEMT devices fabricated with two-step gate recess. MHEMT devices exhibit a good pinch-off characteristic at drain voltage of 1.5 V.

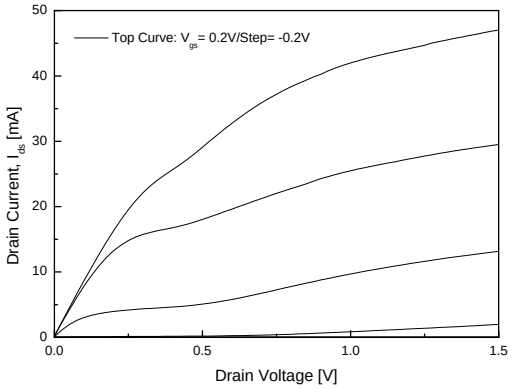

Fig. 3. I-V characteristics for 80nm T-gate MHEMTs.

The drain saturation current, I_{dss}, measured at V_{ds} = 1.5 V and V_{gs} = 0 V is 28 mA. For the 80 nm x 100 μm MHEMT fabricated using wet recess etching, the extrinsic transconductance, g_m, and drain current, I_{ds}, as a function of source-to-gate voltage, V_{gs}, are shown in Fig. 4.

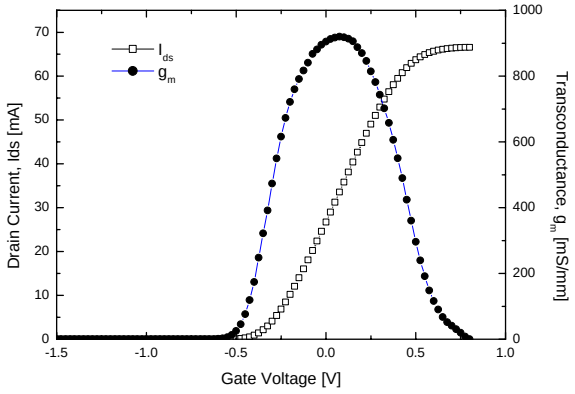

Fig. 4. Transfer characteristics for 80 nm x 100 μm low noise MHEMTs.

The threshold voltage, V_{th} , is defined by a linear extrapolation of the square root of drain current versus gate voltage to zero current. V_{th} was measured as - 0.5 V at V_{ds} = 1.5 V. The typical maximum g_m was measured as 920 mS/mm at V_{gs} = 0.1 V and V_{ds} = 1.5 V.

The *S* - parameters for the 80 nm x 100 μm MHEMT devices were measured on a wafer from 1 to 50 GHz by using a Cascade microwave probe station and an HP 8510C network analyzer. The measured current gain, h_{21}, and MSG/MAG as a function of frequency for MHEMT device are shown in Fig. 5. The cut-off frequency, f_T, was obtained from the extrapolation of h_{21} to unity by using a -20 dB/decade slope, and the maximum frequency of oscillation, f_{max} , was extrapolated from the MSG/MAG. The f_T and f_{max} obtained for 80 nm x 100 μm MHEMT device were 245 GHz and 280 GHz, respectively.

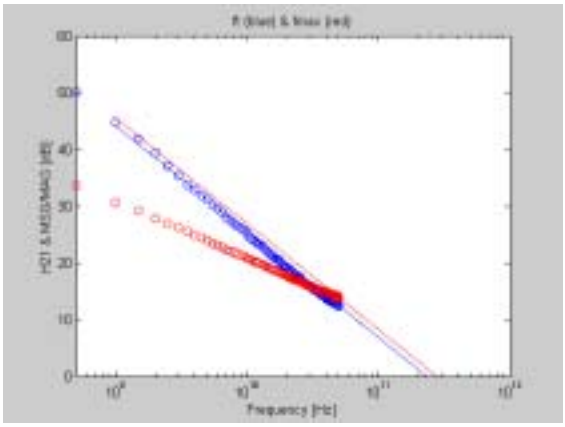

Fig. 5. Typical current gain, h_{21}, and MSG/MAG as a function of frequency for 80nm x 100 μm low noise MHEMTs.

4. Conclusion

The 80nm gate-length low-noise MHEMTs with the T-shaped gate were fabricated using two-step gate recess and characterized for DC and microwave performance. The MHEMT device exhibited the DC output characteristics having an extrinsic transconductance of 920 mS/mm and a threshold voltage of –0.5 V. The f_T and f_{max} obtained for the 80nm x 100 μm MHEMT device were 245 GHz and 280 GHz, respectively. The two-step gate recess process achieved the short recess width of 50nm on the gate of MHEMTs. This gate recess process is applicable to fabricate the high performance MHEMTs.

Acknowledgment

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