Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 956-957

E-8-6

Comparative Study of DC and Microwave Characteristics of 0.12 μm T-Shaped Gate AlGaAs/InGaAs/GaAs PHEMTs Using a Hybrid and Conventional E-beam Lithography Process

Jong-Won Lim, Seok-Won Yoon, Ho-Kyun Ahn, Hong-Gu Ji, Woo-Jin Chang, Jae-Kyoung Mun, and Haecheon Kim

IT Components & Materials Technology Research Division,
IT Convergence & Components Laboratory,
Electronics and Telecommunications Research Institute, Daejeon 305-700, Korea
Phone: +82-42-860-6229 E-mail: jwlim@etri.re.kr

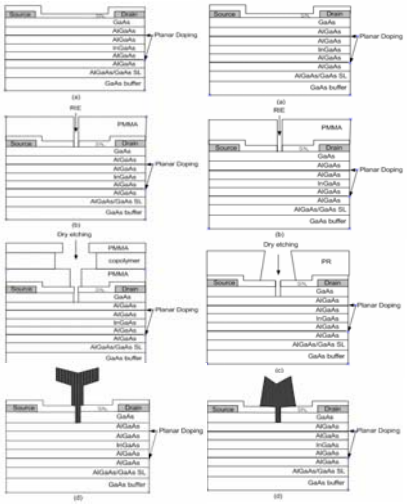
1. Introduction

Pseudomorphic high electron mobility transistors (PHEMTs) are promising devices for millimeter-wave and optical communications systems due to their excellent high frequency and low-noise performance. In order to reduce the gate resistance, T-gates with large cross-sectional area are required. Their fabrication can be either based on electron beam lithography (EBL) with multiple resist layers [1-3] or on optical stepper lithography combined with sidewall spacers. Conventional bi- or tri-layer EBL methods are high-cost and low-throughput process for manufacturing.

In this study, we demonstrate the fabrication of 0.12 μm T-shaped gate AlGaAs/InGaAs/GaAs PHEMTs using a hybrid and conventional EBL process. A hybrid lithography process has been established using high-voltage EBL system and I-line 5X stepper. We report the results of using two different lithography techniques to obtain T-shaped gates with 0.12 μm gate lengths. It will be shown that 0.12 μm T-shaped gate PHEMTs fabricated using this process exhibit good DC and microwave characteristics.

2. Experimental Details

The PHEMT epitaxial structure was grown by molecular beam epitaxy (MBE) on a semi-insulating GaAs substrate and consists of the following layers : 5000 Å GaAs buffer, 30 periods of AlGaAs/GaAs supperlattice buffer, an undoped $Al_{0.23}Ga_{0.77}As$ buffer, silicon planar doping (1×10^{12} cm^{-2}), a 20 Å $Al_{0.23}Ga_{0.77}As$ spacer, a 120 Å $In_{0.2}Ga_{0.8}As$ channel, a 35 Å $Al_{0.23}Ga_{0.77}As$ spacer, silicon planar doping (4.5×10^{12} cm^{-2}), a 250 Å $Al_{0.23}Ga_{0.77}As$ Schottky contact layer. Finally, a 400 Å n-type doped GaAs cap (5×10^{18} cm^{-3}) layer was grown to protect the active layer from the oxidation, causing the creation of defects [2]. The mesa was defined by conventional photolithography. The ohmic contact alloying was performed by two-step annealing, first at 330℃ and then at 380℃, for 20 s each. The steps of the fabrication of conventional and hybrid T-shaped gates using a SiN_x-assisted process are outlined schematically in Fig. 1. A 400 Å SiN_x layer was deposited by PECVD at 260℃ to protect the device and to support the gate. Then, the T-gate footprint patterning was done by EBL using a Leica EBPG 5000 plus system.



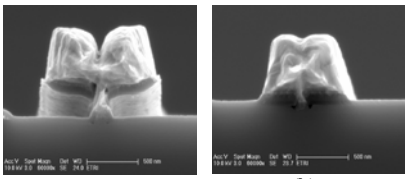
(A) (B)

Fig. 1. Cross-sectional schematic view of 0.12 μm T-gate PHEMTs fabrication process. (A) conventional; (B) hybrid.

The T-gate footprint is written in just a single layer of PMMA. The SiN_x layer was etched by RIE to create a 0.12 μm gate footprint. In case of conventional process, the top of the T-gate was defined by applying EBL to a tri-layer resist [PMMA/copolymer/PMMA]. The top of the T-gate structure which consists of a wide head part and a narrow lower layer (0.3 μm) has been employed taking advantages of its large cross-section area of the gate and mechanically stable structure. In case of hybrid process, the top of the T-gate was defined with a Nikon I-line 5X stepper that can reliably pattern 0.5 μm in a single layer of photoresist. To obtain reproducible gate recess processing, the GaAs cap layer was selectively etched by ICP dry etching using Oxford Plasma Technology Plasmalab System 100™. The GaAs cap layer was selectively etched using BCl_3/SF_6 gas mixtures. The etch rate of GaAs cap layer was 860 $Å/min^{-1}$. After the gate recess, Ti/Pt/Au layers were deposited and lifted-off. Figure 2 shows a SEM image of the cross-section of the fabricated conventional and hybrid processed T-gate PHEMTs taken from an actual devices.

3. Results and Discussion

PHEMTs with source-to-drain spacings of 2.5 μm, source-to-gate spacings of 0.79 μm, gate-to-drain spacings

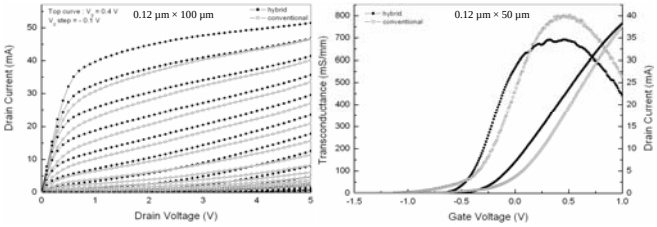


(a) (b)

Fig. 2. SEM images of cross section of real fabricated T-gate PHEMTs. (a) conventional; (b) hybrid.

of 1.59 μm, unit gate widths of 50 μm and two gate fingers, gate lengths of 0.12 μm were fabricated using the single and the tri-layer resist on the PHEMT structure. This asymmetric source and drain structure with shorter gate-to-source separation than gate-to-drain can be applied for reducing the source resistance. The DC and RF characteristics were evaluated by measuring the devices in a HP 4156B DC parameter analyzer and a HP 8510C network analyzer, respectively.

Figure 3(a) shows drain current as a function of source-to-drain voltage (V_{ds}) for 0.12 μm PHEMTs fabricated by conventional and hybrid process. The devices exhibited good pinch-off characteristics. We obtained a pinch-off voltage of V_p = - 0.89 V, and a drain-source saturation current (I_{dss}) of 21 mA at V_{gs} = 0 V and V_{ds} = 5 V for conventional process. In case of hybrid process, the pinch-off voltage of V_p = - 0.62 V, and a drain-source saturation current (I_{dss}) of 29 mA at V_{gs} = 0 V and V_{ds} = 5 V. The extrinsic transconductance (g_m) and drain current (I_{ds}) as a function of source-to-gate voltage (V_{gs}) at 1.5 V of drain voltage were measured and shown in Fig. 3(b). The maximum g_m was measured as 800 mS/mm for conventional process at V_{gs} = 0.44 V and 685 mS/mm for hybrid process at V_{gs} = 0.3 V.



(a) (b)

Fig. 3. (a) Drain current as a function of source-to-drain voltage and (b) the extrinsic transconductance and drain current as a function of source-to-gate voltage for the fabricated 0.12 μm PHEMT device.

The gate-to-drain breakdown voltage curves are shown in Fig. 4. The hybrid processed device has a gate-to-drain breakdown voltage of -6.9 V, as compared to that of -3.4 V for conventional processed device. The breakdown voltage of the hybrid process is larger than that of the conventional process. It is believed that the side-etching length of the hybrid process is larger than that of the conventional process [4].

The RF properties of the fabricated PHEMTs were measured by on-wafer probing. Typical current gain (h_{21}), maximum stable and available gain (MSG/MAG) as a function of frequency for conventional process are shown

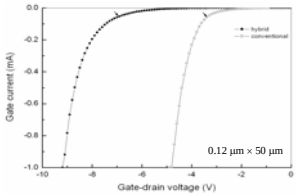
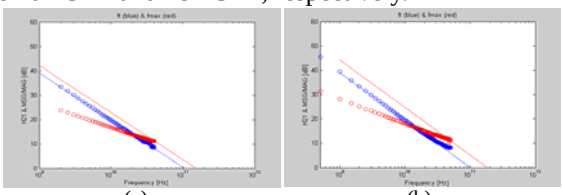


Fig. 4. Gate-to-drain breakdown characteristics for conventional and hybrid processed devices.

in Fig. 5(a). The drain and gate voltages applied in the RF measurements were 1.5 and 0.4 V, respectively. From the measured S-parameters, the small-signal equivalent circuit was extracted using a direct extraction technique and the corresponding f_T and f_{max} were estimated. Both f_T and f_{max} were calculated using the h_{21} and MSG/MAG values by an extrapolation of – 20 dB/decade slope. The current gain cut-off frequency (f_T) was 105 GHz and the maximum oscillation frequency (f_{max}) was 152 GHz. Current gain h_{21} and MSG/MAG as a function of frequency for hybrid process are shown in Fig. 5(b). The extrapolated f_T and f_{max} were 101 GHz and 184 GHz, respectively.



(a) (b)

Fig. 5. Measured current gain and maximum available gain as a function of frequency for the fabricated 0.12 μm PHEMT devices. (a) conventional; (b) hybrid.

The hybrid process result was comparable values than the previously reported values for a conventional PHEMT process [1-3]. This method is promising in solving the problem of yield and throughput compared to conventional gate technology defined via electron beam lithography as well as obtaining a mechanically stable T-gate structure. This hybrid process has been employed for T-gate structures for devices in a program on MMICs for 60GHz pico-cell wireless communications.

4. Conclusions

The fabrication of 0.12 μm conventional and hybrid processed T-gate PHEMTs with the SiN*x* assisted process has been described. To obtain reproducible gate recessing, the GaAs cap layer was selectively etched by ICP dry etching. A hybrid lithography process has been established using EBL and optical lithography. The hybrid process will be able to improve wafer throughput by eliminating the time consuming electron beam lithography step.

References

[1] H. S. Kim, B. O. Lim, S. C. Kim, S. D. Lee, D. H. Shin and J. K. Rhee, Microelectronic Engineering **63** (2002) 417.

[2] J. H. Lee, H. S. Yoon, J. Y. Shim and H. Kim, Thin Solid Films **435** (2003) 139.

[3] J. W. Lim, H. K. Ahn, H. G. Ji, W. J. Chang, J. K. Mun and H. Kim, Jpn. J. Appl. Phys. 43 (2004) 7934.

[4] T. Ohshima, M. Yoshida, R. Shigemasa, M. Tsunotani and T. Kimura, Jpn. J. Appl. Phys. 39 (2000) 5052.