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High-temperature and UV-assisted C-V characterization of GaN MIS structures

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1. Introduction

GaN-based materials have been investigated for realization of devices for high-power electronics. The metal-insulator-semiconductor (MIS) structures are very attractive for high-power devices, because they can reduce gate leakage and enhance the dynamic range of device operation. To realize well-controlled and reliable MIS structures, it is very important to characterize the I-S interface properties including the density distribution of interface states. The capacitance-voltage (C-V) method is generally used for this purpose.

In case of GaN MIS structures, however, it is difficult from room-temperature C-V characterization to obtain the properties of interface states located near midgap or deeper. **Figure 1** roughly shows the energy range of the interface state that one can evaluate from the C-V method. We assumed a typical value of $1x10^{16}cm^{-2}$ as the capture cross section for interface state. The states near midgap or deeper have extremely large time constants for carrier emission at RT. In this case, the charging state is remained almost unchanged during the sweeping of gate voltage even if the interface states have high density. Thus, the RT C-V method can only give the response from the state with a limited energy range shown in Fig. 1(a). A high-temperature condition changes this situation. For example, the C-V result measured at 300°C can reflect the charging and discharging behavior of the states around the midgap of GaN, as shown in Fig. 1(b). For further deeper states, a photo-assisted C-V method is one of the powerful tools for the interface state characterization.

This paper presents high-temperature and UV-assisted C-V characterization of GaN MIS structures, for the understanding of "true" interface properties of widegap semiconductor MIS systems.

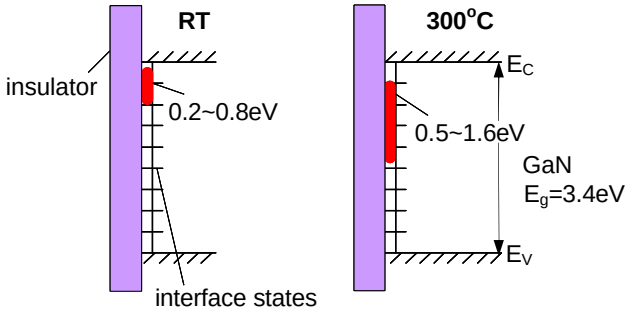


Fig.1 The energy range of the interface state that one can evaluate from the C-V method at (a) RT and (b) 300°C.

2. MIS structure

Figure 2 schematically shows the GaN MIS structure. We used an undoped GaN layer ($n=5x10^{15}cm^{-3}$) grown on sapphire substrates by metal organic vapor phase epitaxy (MOVPE) in the present work.

A device fabrication process started from the deposition of SiO_2 film with a thickness of 15nm by plasma-enhanced CVD. SiH_4 and N_2O were used as source gases, and the deposition temperature was 300°C. A ring shaped ohmic contact (Ti/Al/Ti/Au) was formed on the GaN surface by the EB evaporation and the annealing process at 800°C for 1 min in N_2 atmosphere. Then, a circular Al/Au gate with diameter of 600μm was fabricated on the SiO_2 film. C-V measurements were performed at temperatures from RT to 300°C as well as under UV illumination (wave length: 200-400nm).

3. Results and discussion

Figure 3(a) shows a result of C-V measurement of the SiO_2/GaN sample at temperatures from RT to 300°C. At RT, a plateau region can be seen at the bias from -1.0 to -1.5V. This behavior is often observed for the insulator-semiconductor interfaces where a discrete trap level exists in energy near the bottom of conduction band [1]. The plateau behavior gradually reduced with temperature in the C-V curves, probably due to a low occupation possibility for electrons in the discrete level at higher temperatures. In addition, the flat-band voltage shifted toward positive bias direction with temperature. The reason for this is not clear yet, although mobile charges in the SiO_2 film (ions) may affect the C-V characteristics.

At 200°C and 300°C, we observed a pronounced reduction of the C-V slope. The thermally-stimulated emission rates for electrons at the interface states increase with temperature, leading to the increase in the charge density due to ionization of interface states located even at deeper energies. This can impede the field-effect control of the depletion layer, resulting in decrease in the C-V slope, as shown in Fig. 3(a). In addition, a nearly constant

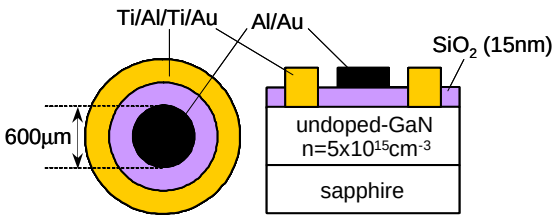
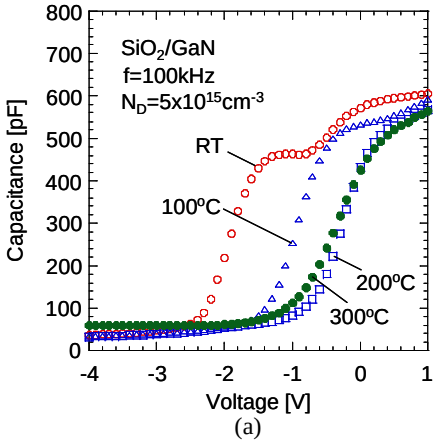
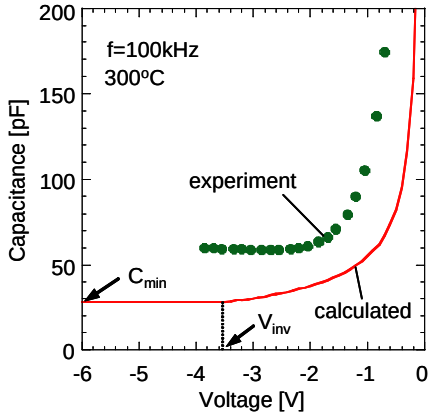


Fig.2 GaN MIS structure



(a)



(b)

Fig.3 (a) C-V characteristics of SiO_2/GaN sample at temperatures from RT to 300°C. (b) An enlarged position of the C-V curve measured at 300°C, together with the calculated one for the surface inversion.

behavior was observed in the deeper bias region in the C-V curve measured at 300°C. Apparently, it seems the well-known effect of minority carrier accumulation at the interface due to strong surface inversion. However, this is not the present case. **Figure 3(b)** shows an enlarged position of the C-V curve measured at 300°C, together with the calculated one for the surface inversion. The experimental values of the inversion voltage and the minimum capacitance are very different from theoretical ones. One of the possible reasons for this constant C-V behavior is that a large amount of charges induced by ionization of interface states near midgap could terminate the electric force lines from the gate plate, thereby blocking the motion of the depletion layer. Thus, we can observe some specific C-V characteristics arising from deeper states at higher temperatures.

Figure 4 shows C-V curves measured under UV illumination (wave length: 200-400nm) at RT. First, the gate voltage was swept from positive to negative bias direction under dark. The UV light was turned on at -9V and kept to -10V. Then the light was turned off, and the gate bias was swept back toward the positive direction. As expected, a rapid increase in capacitance after turning on the UV light is probably due to accumulation of holes at the SiO_2/GaN interface. However, these holes disappeared

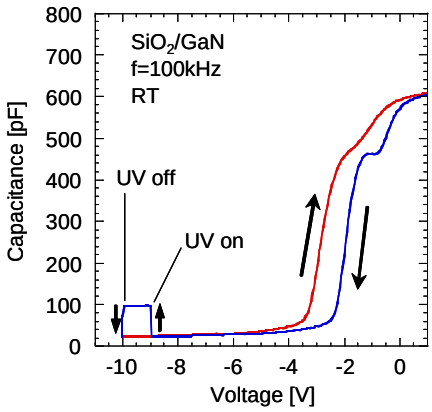
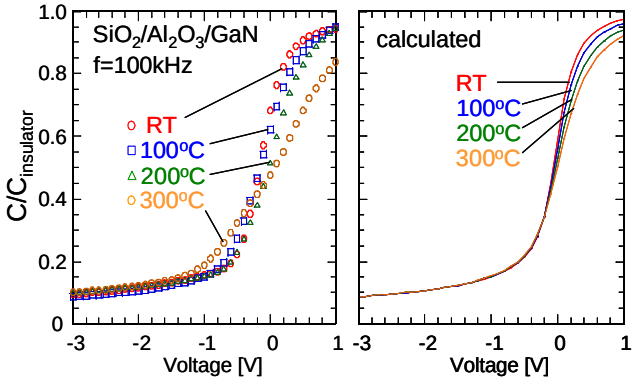


Fig.4 C-V characteristics under UV illumination at RT.



(a) (b)

Fig.5 (a) C-V characteristics of SiO_2/Al_2O_3/GaN sample at temperatures from RT to 300°C and (b) theoretical curves.

promptly after turning off the UV light, indicating interface states rapidly compensated the UV-generated holes. In addition, we observed the shift of the flat-band voltage in the C-V curve after the UV illumination. The result obtained predicted the existence of high-density interface states in energies from midgap to the top of valence band, in agreement with the high-temperature C-V results.

To improve interface properties of the SiO_2/GaN structure, an ultrathin Al_2O_3 layer was involved at the interface. Firstly, the GaN surfaces were treated in N_2 radical in a MBE chamber. Then, thin Al layer with a nominal thickness of 1 nm was deposited at RT using K-cell, followed by the in-situ anneal at 700°C for 10 min.

Figures 5 (a) and (b) show the C-V results for the SiO_2/Al_2O_3/GaN sample and the calculated curves, respectively. In comparison with the SiO_2/GaN sample, the plateau region and the flat-band voltage shift were not observed in the SiO_2/Al_2O_3/GaN structure. In addition, the C-V curves measured at the temperatures up to 200°C were almost the same with theoretical curves. These results indicated that the ultrathin Al_2O_3 layer could reduce interface states effectively. However, the decrease in the C-V slope appeared at 300°C, suggesting the effect of the Al_2O_3 control layer is not sufficient, in particular on the states in deeper energies.

[1] T. Hashizume and R. Nakasaki, Appl. Phys. Lett. **80**, 4564 (2002).