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Device Isolation by Plasma Treatment for Planar Integration of E/D-mode AlGaN/GaN HEMTs

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1. Introduction

Owing to the wide bandgap of III-nitride materials, depletion-mode (D-mode) and enhancement-mode (E-mode) AlGaN/GaN HEMTs are attracting great interests in digital high temperature ICs [1, 2]. E/D-mode HEMTs integration have been fabricated using recess gate [1] and fluoride plasma treatment techniques [2], both of which used mesa etching to achieve the active device isolation. To achieve high density and high uniformity in the E/D HEMTs integration, the three-dimensional mesas impose serious limits to photolithography and interconnect. In this work, the fluoride plasma treatment is adopted in two separate steps to achieve two objectives: 1) active device isolation; and 2) threshold voltage control for E-mode HEMT formation. Therefore, a planar integration for E/D HEMTs is demonstrated without any mesa and gate-recess etching.

2. Devices Fabrication and Characterization

The AlGaN/GaN HEMT structure used in this work is grown on (0001) sapphire substrates in an Aixtron AIX 2000 HT metal-organic chemical vapor deposition (MOCVD) system. The HEMT epitaxial structure is similar to that used in our previous work [3], with an AlGaN barrier of 26 nm.

The planar integration process flow is illustrated in Fig. 1. After the source/drain ohmic contacts of E/D-mode devices are formed simultaneously by e-beam deposition of Ti/Al/Ni/Au and rapid thermal annealing (RTA), the active regions for both E/D-mode devices are patterned by photolithography followed by CF_4 plasma treatment (300 W for 100 seconds) in an STS reactive ion etching (RIE) system, as shown in Fig. 1 (a) and (b). The isolation regions are the locations where large amount of F^- ions are incorporated in the AlGaN and GaN layers near the surface, and deplete the 2DEG in the channel. The D-mode HEMTs' gate electrodes are then patterned by e-beam evaporation of Ni/Au and lift-off (Fig. 1(c)). Next, E-mode HEMTs' gate electrodes and interconnections are defined. Prior to deposition of Ni/Au, the gate regions of E-mode HEMTs are treated by CF_4 plasma at 170 W for 150 seconds, shown in Fig. 1(d). This plasma treatment performs the function of converting the treated devices from D-mode to E-mode HMET [3]. A 200 nm-thick SiN passivation layer is deposited by PECVD and the probing pads are opened. Then the whole sample is annealed at 400ºC for 10 min to repair the plasma induced damage in the AlGaN layer and the channel of E-mode HEMTs (Fig. 1(e)) [3]. As a comparison, the D-mode devices are also fabricated on the same substrate by standard process, in which ICP-RIE (inductively coupled plasma RIE) is used to define mesa as active region. For the direct-coupled FET logic (DCFL) inverter shown in this paper, the E-mode HEMT driver is designed with gate length, gate width, G-S and G-D spacing of 1.5, 50, 1.5 and 1.5 μm respectively; the D-mode HEMT load is designed with gate

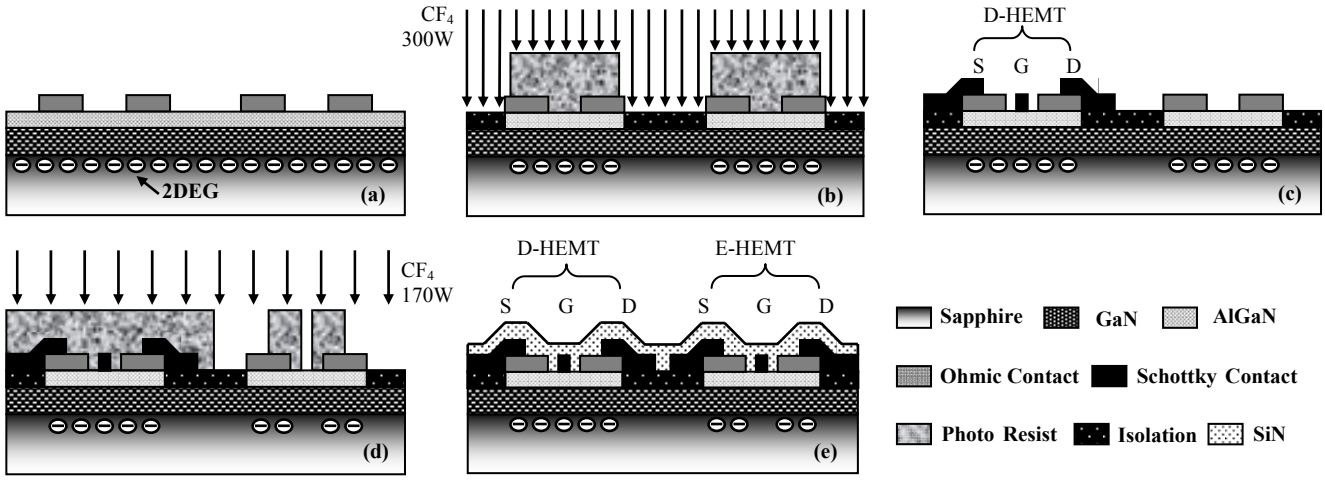

Fig. 1 Schematics showing the process flow of E/D mode HEMTs: (a) Ohmic contact; (b) Active region definition by plasma treatment; (c) D-mode gate formation; (d) E-mode gate definition and plasma treatment; (e) SiN passivation.

length, gate width, G-S and G-D spacing of 4, 8, 3 and 3 μm, yielding a ratio β of 16.7, where β equals $(W_D/L_D)/(W_E/L_E)$. The discrete E/D-mode HEMTs with gate dimension of 1.5 μm x 100 μm are fabricated for characterizations.

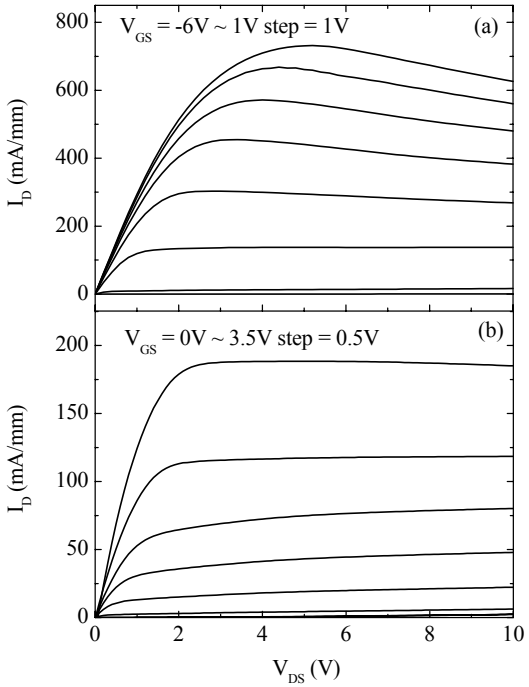

Fig. 2 DC output characteristics of (a) D-HMET and (b) E-HEMT by planar process

For the E/D-mode HEMTs fabricated by the planar process, the output characteristics are plotted in Fig. 2. The peak current density for D-mode and E-mode HEMTs are about 730 and 190 mA/mm. Fig. 3 shows the transfer characteristics comparison between planar and standard process. It can be seen that the drain leakage current for planar process is ~0.3 mA/mm, reaching the same level as the devices fabricated by standard mesa etching. It is proved that, compared with the standard mesa process, the fluoride-based plasma treatment can achieve the same level of active device isolation, enabling a complete planar integration process. The E-mode HEMTs exhibit smaller transconductance (g_m) compared to D-mode devices, due to the incomplete recovery of the plasma induced damage [3]. The fact that the sample has been through a thermal annealing at 400ºC indicates that good thermal stability is expected at temperature at least up to 400ºC.

An E/D mode HEMTs DCFL inverter fabricated by the planar process is characterized in Fig. 4. High and low logic levels are 3.3 and 0.45 V, respectively. By defining the values of input low and high at the unit gain points, the low and high noise margins are 0.34 and 1.47 V. The leakage current with E-mode device pinch-off is about 3 μA, which is consistent with the discrete devices' results.

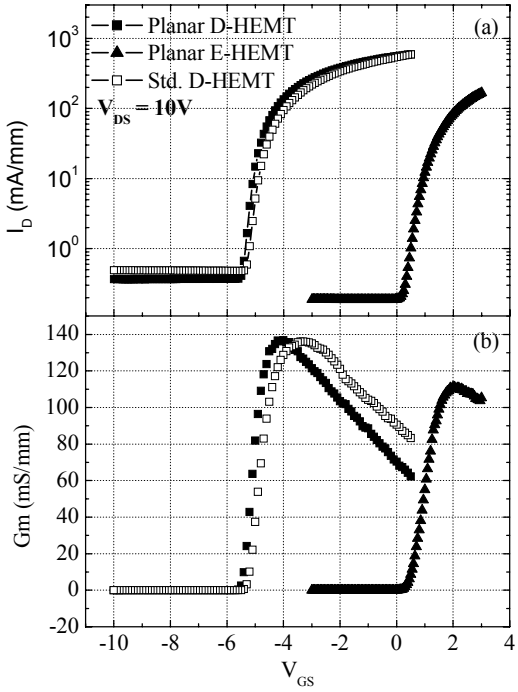

Fig. 3 Transfer curves comparison between planar and standard process: (a) drain current and (b) g_m comparison.

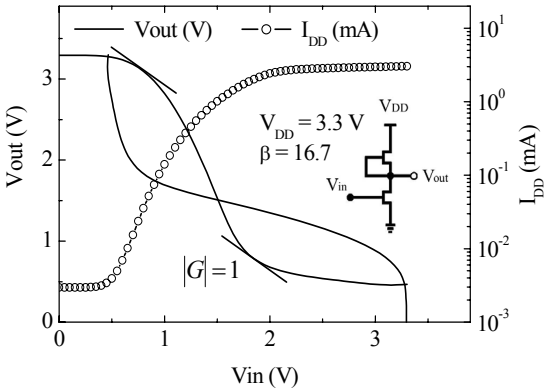

Fig. 4 Static voltage transfer characteristics of an E/D HEMT inverter fabricated by planar process.

3. Conclusions

A new planar process for integration of AlGaN/GaN HEMTs is demonstrated based on fluoride plasma treatment. Without any dry etching for mesa formation and gate-recess, the plasma treatment can achieve the same isolation results between active devices. The plasma treatment can also be used to convert D-mode HEMTs to E-mode. The E/D-mode DCFL inverter has been fabricated using this new technique, in which the whole process is conducted on a pure planar surface.

References

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