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ICP Reactive Ion Etching with $SiCl_4$ Gas for Recessed Gate AlGaN/GaN HFET

K. Matsuura[1], D. Kikuta[1], J.-P. Ao[1], H. Ogiya[2], M. Hiramoto[2], H. Kawai[3] and Y. Ohno[1]

Institute of Technology and Science, The University of Tokushima[1]
2-1,Minami-josanjima, Tokushima 770-8506, JAPAN
Phone&Fax: +81-88-656-9690, E-mail address: matsuura-k@ee.tokushima-u.ac.jp
SAMCO Inc.[2], 36, Waraya-cho, Takeda Fushimi-ku, Kyoto 612-8443, JAPAN
POWDEC K. K.[3], 739, Ichizawa cho, Asahi-ku, Yokohama-shi, Kanagawa 241-0014, JAPAN

1. Introduction

HFETs (Heterostructure Field Effect Transistors) with short channel lengths are being developed on gallium nitride for high frequency applications[1]. In these devices, the gate AlGaN layer must be thin enough to avoid short channel effects, while the access regions must remain relatively thick to keep parasitic resistances at a low level. To fully realize the HFET structure, gate recess etching of the AlGaN layer with a controlled etch rate and no process damage are required [2].

In this paper, we report ICP reactive ion etching (RIE) with $SiCl_4$ gas, which has shown very low etching rate and almost no damage on recessed gate AlGaN/GaN HFETs.

2. Experiments

a. Etching Characteristics

A commercial ICP etching machine (Samco RIE-200-iPG) was used for the experiments. Typical etching conditions were as follows: ICP power of 50W, bias power of 20W, $SiCl_4$ pressure of 0.25Pa, and flow rate of 3 sccm. Etching experiments were carried out on an undoped GaN epi-layer. The etched depth was measured with an atomic force microscope (AFM). An etching rate of 1.2 nm/min was obtained with an etching start offset time of 52sec, which corresponds to 1.0nm GaN thickness. (Fig.1)

The AFM images of the GaN surfaces before etching and after 30min (38nm) etches are almost identical. Root mean square (RMS) values were 0.40nm for the un-etched sample and 0.41nm for the etched sample. These facts indicate the smoothness of the etched surface and high uniformity of the etching. (Fig.2)

b. Device Fabrication

The etching technique was applied to the fabrication of a recessed gate AlGaN/GaN HFET. (Fig.3) The AlGaN/GaN epi-layer was grown on a *c*-plane sapphire substrate, with a AlGaN layer thickness of 28nm. After the isolation etching by RIE with BCl_3, the ohmic electrode was formed by sputtering (Ti/Al/Ti/Au:50/200/40/40nm) and was annealed at 850C in N_2 for 30 seconds. With a photo-resist mask, the gate regions were etched for ten minutes under the conditions mentioned above. The gate metals (Ni/Au:30/150nm) were then evaporated through the photo-resist pattern.

c. Device Characteristics

From C-V measurement of L/W=100 μm/200 μm FAT-FET structure, the AlGaN layer thicknesses were 29.1nm for the un-etched sample and 19.7nm for the etched sample. Here, we used the capacitance value at V_G=0V and assumed 9.5 for the relative dielectric constant for the AlGaN layer. From the C-V measurement, the etch depth was determined to be 9.4nm, which is a little smaller than the expected value of 10.8nm from the data on GaN. We suspect that the difference was due to the offset time between the AlGaN and GaN, not the difference in the etching rate.

The I_D-V_D characteristics for the recessed gate FETs showed nothing peculiar. The differences found in the HFET with recess etching can be explained by the AlGaN thickness variation and the threshold voltage shift (Fig.4), which is consistent with the value calculated from the thickness variation.

Gate leak current at negative gate bias showed almost no change. At positive gate bias, the current rose sharply with the n-value of 1.68 for the etched sample, while the n-value was 4.09 for the un-etched sample. This may be caused by the removal of some natural oxide layer on the as-grown AlGaN. (Fig.5)

The channel electron drift mobility was obtained from the gate capacitance and transconductance of the FAT-FET at low V_D. (Fig.6) Again, the values showed almost no degradation.

3. Conclusions

We obtained a low etching rate of 1.2nm/min in ICP reactive ion etching with $SiCl_4$. The recessed gate AlGaN/GaN HFETs were made using ICP etching with $SiCl_4$. These HFETs have shown almost no degradation in their electrical characteristics. We believe that ICP-RIE with $SiCl_4$ will be suitable for the gate etching for AlGaN/GaN FETs.

Acknowledgements

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[References]

[1] U.K.Mishra, P.Parikh, and Y.-F.Wu, "AlGaN/GaN HEMTs-an overview of device operation and applications," Proc. IEEE, vol.90, pp.1022-1031, June 2002

[2] Y.Ando, Y.Okamoto, T.Nakayama, H.Miyamoto, T.Inoue, M.Kuzuhara, "12W/mm Recessed-Gate AlGaN/GaN Hetero junction Field-Plate FET" ,in IEDM Tech. Dig, 2003, pp.563-566

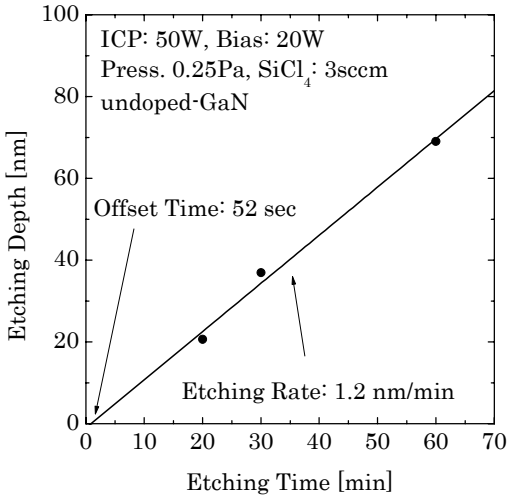

Fig.1 Etching rate experiment on undoped GaN

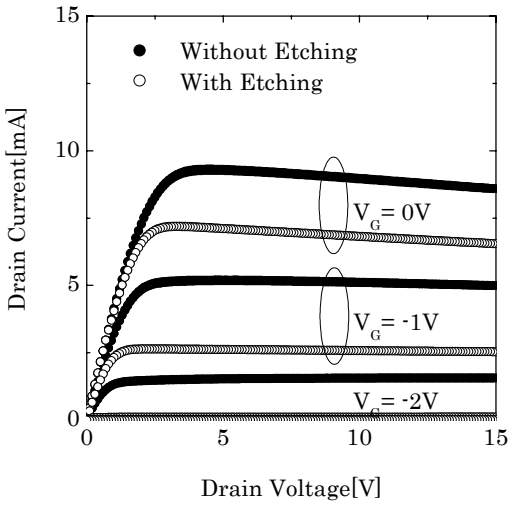

Fig.4 I_D-V_D characteristics of un-recessed and recessed gate HFETs. The gate length is 2μm and width is 50μm.

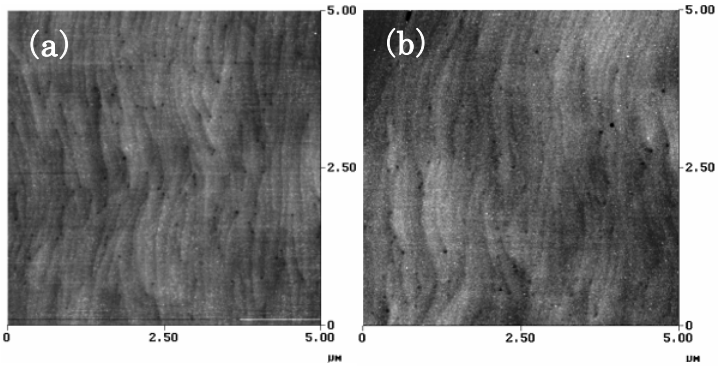

Fig.2 AFM image of surfaces of GaN (a)before etching and (b)after etching for 30min with the etch-depth of about 38nm.

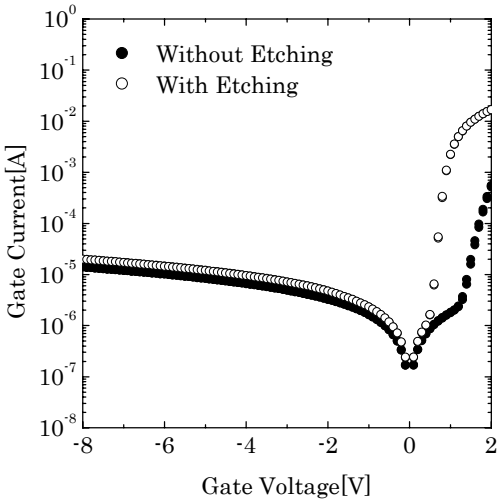

Fig.5 I_G-V_D characteristics of un-recessed and recessed gate HFETs. FET size is the same as those shown in Fig.4.

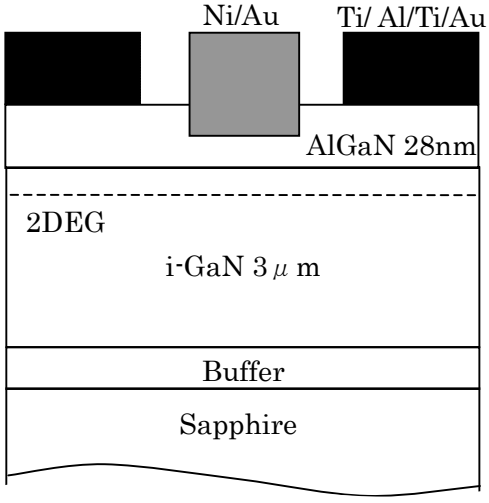

Fig.3 Schematic cross-section of recessed gate AlGaN/GaN HFET.

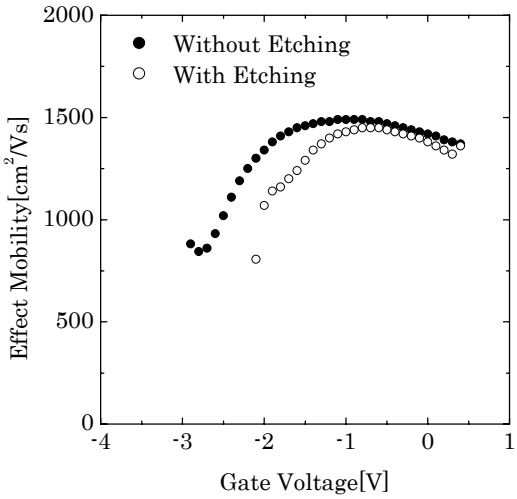

Fig.6 Effective electron drift mobility for the FETs. Mobility was obtained from the ratio of I_D and the carrier concentration at the gate voltage. The carrier concentration was calculated by integration of the capacitance. The drain bias was 0.1V.