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Overview and Future Challenge of FeRAM Technologies

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1. Introduction

As the semiconductor technology moves toward the 65- and 45-nm nodes, the role of nonvolatile memories embedded in system-on-a-chips (SoCs) is becoming extremely important [1]. Especially in ferroelectrics, bismuth-layered perovskite materials such as $SrBi_2Ta_2O_9$ (SBT) [2] can provide SoCs with fast read/write speed, low-voltage and fatigue-free memory performances. Until now, however, ferroelectric random access memory (FeRAM) technology has been two or three generations behind the leading-edge CMOS technology. In addition, the read cycle endurance of FeRAM, typically less than 10^{12} cycles, is not enough to work in SoCs. Now therefore, we need adventurous technology transition in FeRAM materials, processing and readout scheme to catch up with the leading-edge CMOS.

In this paper, we give overview of the current status of the FeRAM technology. Future challenges facing the FeRAM technology are also described.

2. Process Technology

Traditionally, process compatibility of the FeRAM technology has allowed successful implementation of FeRAM in CMOS devices without any modifications to the circuit designs (Fig. 1). In a 0.6-μm FeRAM, a planar capacitor technology was used together with a spin-coat technique. In a 0.18-μm FeRAM, a planer capacitor enclosed in a hydrogen barrier is stacked on a pass transistor and thereby withstands hydrogen treatments during the CMOS back-end process [3]. The memory cell size is then dominated by the capacitor area. Because the planar capacitor is not allowed for much tighter density transistors of a 130-nm FeRAM, a three-dimensional (3-D) capacitor structure was introduced to minimize the footprint. Then a metalorganic chemical vapor deposition (MOCVD) technique was used to form a uniform 3-D ferroelectric film on a topographic electrode inside a capacitor well. At the 65-nm node and beyond, ferroelectric films have to be formed at temperatures lower than 500°C because higher process temperatures will cause an anomalous increase in the sheet resistance of nickel-silicide (NiSi) contact layers for ultra-shallow junctions [4]. When an SBT film is annealed at temperatures lower than 650°C, however, an undesired phase, *i.e.* a fluorite phase, appears and never converts to the perovskite [5]. This dilemma for FeRAM scaling has been solved by choosing $Bi_4Ti_3O_{12}$ (BIT) as a capacitor dielectric. A BIT capacitor deposited at temperature less than 500°C by MOCVD exhibits no fluorite phase and resulted in a large remnant polarization ($2P_r$) of 25.7 μC/cm^2 after annealing at 500°C (Fig. 2).

3. Non-Destructive Readout Operation

Typically, a memory cell of FeRAM consists of a pass transistor and a ferroelectric capacitor (*1T1C*) as shown in Fig. 3(a), in which a binary polarization state is stored. According to a conventional readout scheme, the stored polarization is switched and subsequently rewritten to restore the switched polarization [6]. As the readout operation is repeated, the polarization switching causes ferroelectric fatigue. To avoid fatigue in read operation, ferroelectric gate transistors without polarization switching have been investigated [7]-[10]. For example, a metal-ferroelectric-semiconductor (MFS) structure can modulate the channel conductance according to the direction of the stored polarization in the ferroelectric gate. The stored datum is then readout by sensing the drain-source current. Since no bias is applied to the ferroelectric during the readout operation, polarization switching never occurs. However, this approach requires significant changes in the CMOS device structure.

We have proposed a non-destructive readout (NDRO) technique which can be realized by existing FeRAM technologies [11]-[12]. In the NDRO technique, a ferroelectric gate transistor is composed by connecting a gate electrode of a readout transistor and a ferroelectric capacitor (Fig. 3 (c)). During a readout operation (Fig. 4(a)), a small readout voltage, V_{RD}, is applied to the top electrode so as to transfer the polarization charge on the ferroelectric capacitor to the intermediate gate electrode of the readout transistor. The application of V_{RD} causes a slight flip of polarization, but never switching. Then, the stored datum is readout by sensing the drain-source current. After reading, the slightly flipped polarization is automatically restored by removing V_{RD} (Fig. 4(b)). Finally, a residual voltage on the intermediate gate electrode of the readout transistor is removed by turning the reset transistor on (Fig. 4(c)). A test structure fabricated from a 0.18μm FeRAM process reveals that the NDRO works out perfectly even after 10^{11} cycles of read operation (Fig. 5). We expect this stable readout would continue up to 10^{16} cycles.

4. Conclusion

We have demonstrated some possible solutions for the FeRAM scaling dilemma. We believe these approaches will make the FeRAM technology more attractive for use in the leading-edge CMOS.

References

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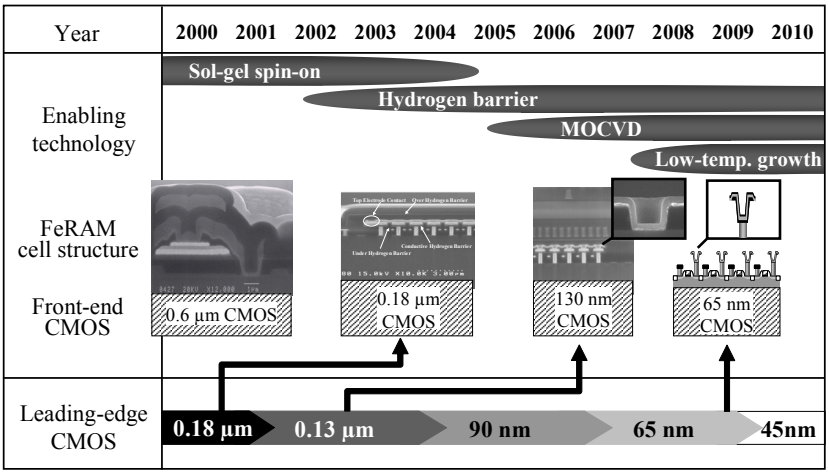

Fig. 1 Technology trend of embedded FeRAM.

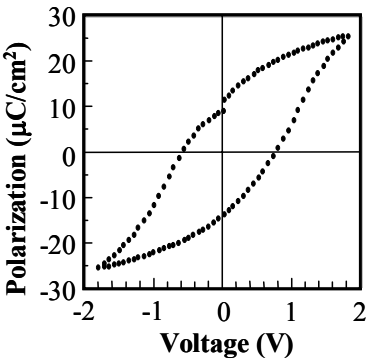

Fig. 2 *P-V* hysteresis curve of a BIT capacitor

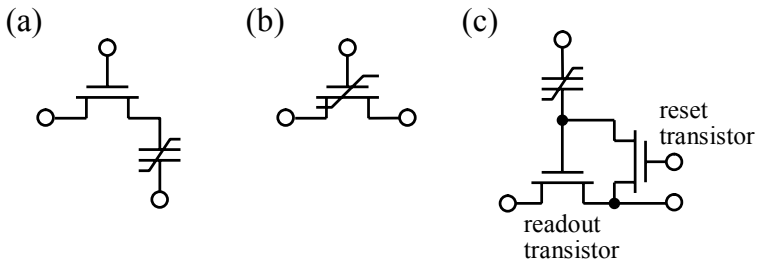

Fig. 3 Memory cell architectures for (a) a 1T1C structure, (b) a MFS cell, and (c) an NDRO cell.

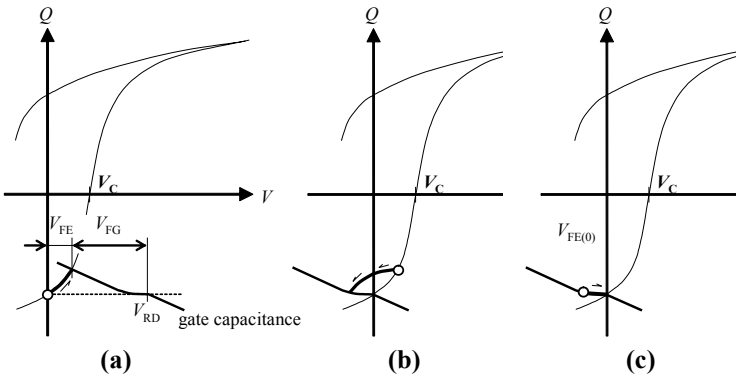

Fig. 4 Portion of a *Q-V* hysteresis curve overlaid with the gate capacitance at (a) readout operation, (b) removal of V_{RD}, and (c) reset operation.

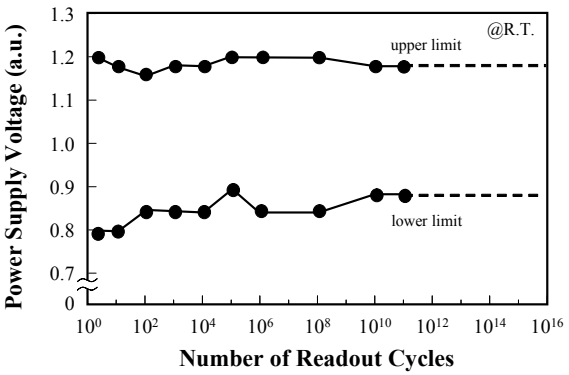

Fig. 5 Operational power supply voltage range as a function of the number of readout cycles.