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Full-Bit Functional, High-Density 8Mb 1T-1C FRAM Embedded Within a Low-Power 130nm Logic Process

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Abstract

We report the electrical properties of a full-bit functional 8Mb 1T-1C Embedded Ferroelectric Random Access Memory (eFRAM) fabricated within a low-leakage 130nm 5LM Cu interconnect CMOS logic process. To increase manufacturability and reliability margins, we have introduced a single-bit substitution methodology that replaces bits at the low-end of the original distribution with redundant elements leading to an increased signal margin. Further, we have fabricated a Digital Signal Processor (DSP) using the eFRAM process flow and have shown that the operating frequency is nearly the same relative to the CMOS baseline. With the development of logic-compatible eFRAM, ***we have created a technology platform that enables ultra- low-power devices.***

1. Introduction

High-density eFRAM offers cost-effective non-volatile memory functionality that complements advanced logic devices by adding distinct capabilities including high-endurance data storage, fast-write data protection, "instant-on", and extended battery life. eFRAM operates at low voltage (1.5V) and, unlike floating-gate devices, does not require power-consuming charge pumps. In recent years, several groups have reported dramatic FRAM cell size reductions and bit reliability improvements[1-5]. We report both a full-bit functional 8Mb eFRAM and a novel weak bit substitution approach to increase signal margin.

2. Integration Approach

The eFRAM module is formed between the CONT and MET1 levels of a standard logic flow as described in [5]. Briefly, this involves the following: capacitor stack deposition; a single-mask stack etch to remove the Ir/IrO_x top electrode, PZT, Ir bottom electrode and TiAlN diffusion barrier layers; a second mask to define the bi-level VIAs that connect MET1 either to the top of the capacitor or to the W plug. The integration process then continues along the standard logic flow. Because of the additional VIA, the contact resistance for the eFRAM flow is 10 ohms larger than that obtained for the CMOS flow.

An operating frequency comparison between DSPs fabricated using the CMOS baseline and those formed using the eFRAM process is shown in Figure 1. Measurement results indicate that the DSP design created using the standard 130nm logic library maintains yield and performance when fabricated with the eFRAM process.

3. Array Properties

An optical micrograph of the 8Mb eFRAM is displayed in Figure 2. The eFRAM array and supporting circuits, without the bondpads, have an area of $12mm^2$ (~$660kb/mm^2$). Device features are summarized in Table 1.

The measured bit distribution histogram for the eFRAM array, following 5LM Cu metallization, is shown in Figure 3. Approximately 165mV separation is achieved between the "0" and "1" average bit values for the non-delayed (~100ns) read case and roughly 125mV separation for delayed (1s) read. Ferroelectric domain back-switching and relaxation effects, which occur in the ms regime, account for the difference between the two curves. This signal margin is sufficient to achieve full distribution separation. However, we have found that the tail bits are spatially localized within the array and we believe that further process/design optimization will lead to an increased signal margin. Note that the bit distribution remains nearly constant up to 85ºC operation, as shown in Fig. 4, indicating the temperature stability of the memory element [5].

With the implementation of a novel FRAM-based, micro-redundancy routine [6], weak bits, which reduce signal margin, are replaced with redundant elements (Figure 5). Using this approach, we can increase both the sensing margin and improve device reliability enabling a production-worthy, high-density eFRAM technology. Full-chip operation down to a core voltage of 1.1V is achieved as shown in Figure 6.

In summary, we have demonstrated the operation of a high-density embedded FRAM, compatible with advanced DSPs, that enables ultra-low-power devices for use in system-on-chip applications.

References

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Table I Device features tabulated for the 8Mb, 1T-1C embedded FRAM device. The FRAM array and plate line operate off of a 1.5V power supply to ensure compatibility with a low-power, low-cost, single-oxide CMOS process.

Device Features	
FRAM Size	8Mb
FRAM Density	~ 700kb/mm^2
FRAM Configuration	1T-1C or 2T-2C
Architecture	Folded Bit Line
Plate Line Voltage	1.5V
Word Line Voltage (write back)	2.3V
Active / Sleep Current	< 15mA / 5µA
Bit Line Capacitance	240fF
Reading Methodology	After Pulse
Read Access	45ns
Cycle Time	60ns
Column / Row Redundancy	32 / 16
Random Bit Repair	128
Zero-cancellation	Partial

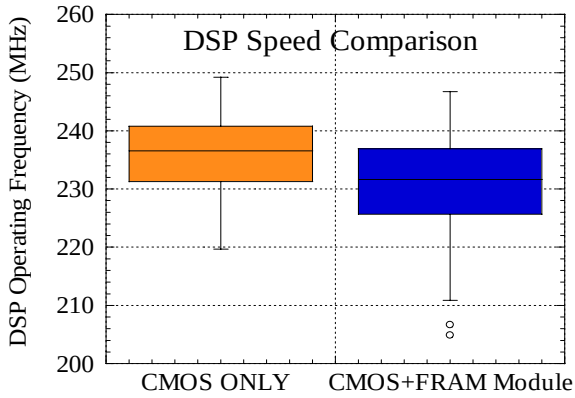

Fig. 1 DSP operating frequency comparison using either the CMOS baseline (~236 MHz) or eFRAM (~232 MHz) process flows.

Standalone Area
16.8 mm^2

Embedded Area
< 12 mm^2

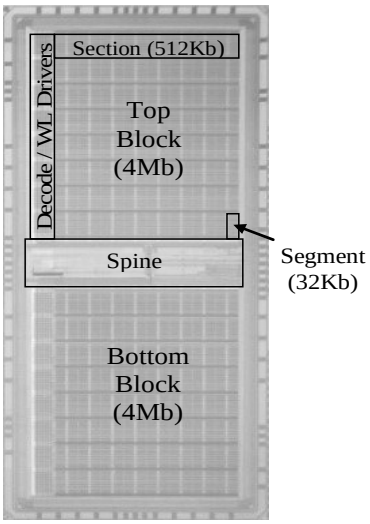

Fig. 2 Annotated die picture showing the two 4Mb eFRAM blocks with the control spine, decoder, and 32kb segments labeled.

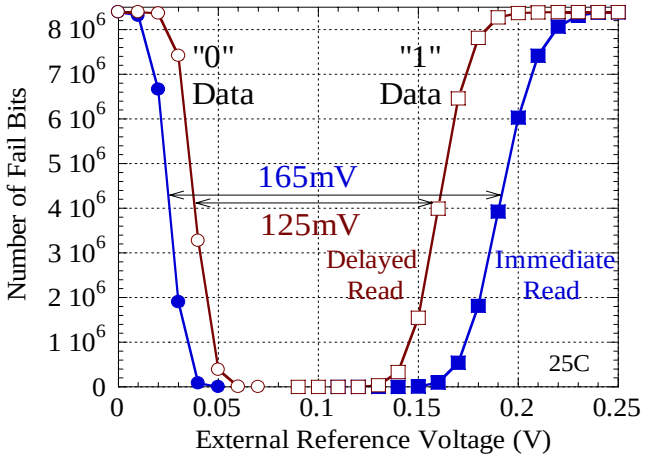

Fig. 3 Bit distribution (linear scale) showing data separation for both immediate-read (~100ns) and delayed-read (~1s) operation.

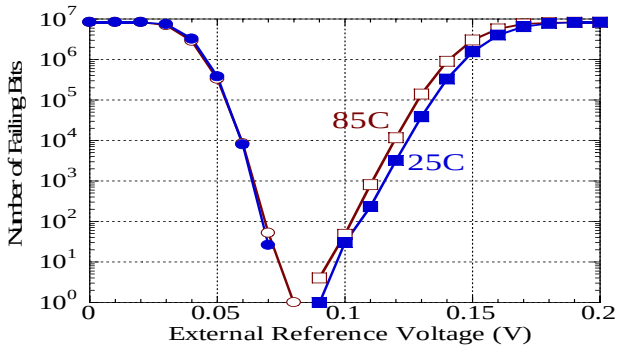

Fig. 4 Bit distribution (logarithmic scale) showing delayed-read data separation for both room-temperature (25ºC) and elevated temperature (85ºC) operation.

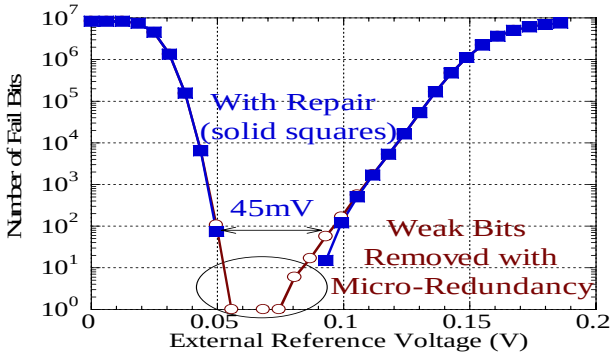

Fig. 5 Bit-distribution (logarithmic scale) showing an increased signal margin through the use of a micro-redundancy algorithm which replaces the weakest bits.

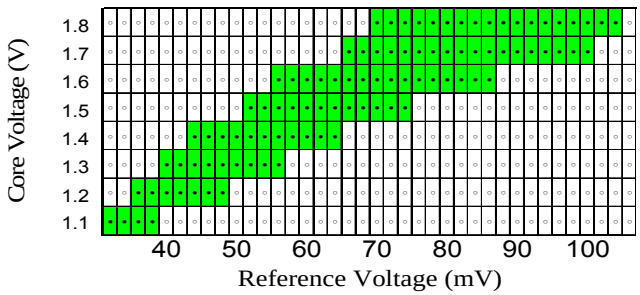

Fig. 6 Full-chip operating regime (fill-in boxes) achieved for core voltages ranging from 1.1V to 1.8V. The core voltage corresponds to both Vdd and the plate line voltage.