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# Robust 2-D Stack Capacitor Technologies for 64Mb 1T1C FRAM

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## 1. Introduction

FRAM (Ferroelectric Random Access Memory) has been pursued as a future mobile memory due to its ideal memory properties [1]. As the cell size of FRAM scales down for high density FRAM, ferroelectric MIM cell capacitor scales down in proportion vertically and horizontally [2]. It is well known that interfacial abnormal layer is openly produced between ferroelectric PZT film and electrode and plays a crucial role in the degradation of ferroelectric capacitor at reduced PZT film thickness. It is also true that ferroelectric capacitor etching causes plasma and charging damage on a ferroelectric capacitor and degradation from capacitor etching is getting worse as capacitor size is getting smaller. Thus, developing capacitor module technologies such as robust PZT film technology at nm scaled PZT thickness and damage minimized ferroelectric capacitor etching technology are crucial for the success of high density 1T1C FRAM. Recently, we have developed a novel capacitor thin film process and capacitor etching technologies from which 64Mb 1T1C FRAM at 180 nm technology node has been successfully demonstrated where robust 0.28 $\mu m^2$ sized 2-dimensional capacitor with 70 nm thin MOCVD PZT were realized.

In this paper, we will discuss key advanced capacitor module technologies for 64Mb 1T1C FRAM and will discuss device electrical results of 64Mb 1T1C FRAM.

## 2. Key capacitor module technologies for 64Mb 1T1C FRAM

Figure 1 shows V-SEM image of unit cell of our 64Mb 1T1C FRAM. Table 1 lists device and process features of 64Mb 1T1C FRAM. Cell size and capacitor size are 0.48 $\mu m^2$ and are 0.28 $\mu m^2$ respectively. 70 nm thick MOCVD PZT and SRO/Ir top electrode were used for robust 0.28 $\mu m^2$ sized 2-D capacitor. Single hard mask etching was used for safe isolation of cell capacitors spaced by 180 nm in width. $Al_2O_3$ hydrogen barrier technology was used for preventing hydrogen related damage.[3] Al-1 plate line scheme was newly adopted for avoiding high aspect ratio plate line contact fill process. Process details for 64Mb 1T1C FRAM are discussed in elsewhere [4].

In order to obtain best ferroelectric properties at reduced 70 nm thick ferroelectric PZT film, various process conditions of PZT deposition and top SRO electrode were tested. Figure 2 shows hysteresis and leakage characteristics of ferroelectric capacitors with 70 nm thick MOCVD PZT receiving different MOCVD PZT deposition conditions, A and B which differ in both the temperatures of substrate and the temperature of carrier gas of MOCVD PZT source. Ir and SRO/Ir were applied for bottom electrode and top electrode respectively for the test. Figure 3 shows retention characteristics of ferroelectric capacitors with different deposition conditions, A and B. Figure 4 shows step by step 2Pr degradation of ferroelectric capacitors with different conditions, A and B. It is obvious that ferroelectric capacitor receiving B-process condition shows better retention and less integration induced degradation. It is reasoned that process condition B not only minimizes interface abnormal layer between bottom electrode Ir and MOCVD PZT, but also produces uniform and favorable directional PZT ferroelectric film.

In order to optimize interface characteristics between PZT and top electrode, SRO thicknesses were varied by changing the system power and process time. As indicated in figure 5, abrupt increase of leakage current was monitored at the SRO thicknesses above a certain boundary thickness indicating that too excess SRO electrode causes the degradation of interface between PZT and top electrode. Thus, applying optimal thickness of SRO electrode is crucial to obtain good interface between top electrode and MOCVD PZT.

Effect of capacitor etching on the degradation of 0.28 $\mu m^2$ sized 2-D stack ferroelectric capacitor were studied by varying plasma type of single hard-mask etching and by varying temperature of top and bottom electrode etching. Figure 6 show DC leakage current and 2Pr characteristics of ferroelectric capacitors etched with different conditions, C and D. Recovery anneal in oxygen ambient above 500$^oC$ was applied after capacitor etching. Detailed etching conditions for condition-C and -D and resulting etching slopes are listed in Table 2. It is clear that both plasma type of hard mask etching and substrate temperature for electrode etching greatly influence leakage current of ferroelectric capacitor.

Figure 7 shows hysteresis of ferroelectric capacitor of 64Mb 1T1C FRAM after full integration using above optimized ferroelectric capacitor stack deposition and capacitor etching technologies. 2Pr of 40 $\mu C/cm^2$ was obtained and is amount to 90% of 2Pr at as-received state. It can be concluded that by newly developing advanced MOCVD PZT process technology and capacitor etching technology, robust ferroelectric capacitor properties on 0.28 $\mu m^2$ sized 2-D capacitor was successfully obtained.

## 3. Device performances of 64Mb 1T1C FRAM

Figure 8 shows microscopic chip image of our experimental 64Mb 1T1C FRAM. Figure 9 shows shmoo plot of

64Mb 1T1C FRAM. 80 ns speed was achieved at 1.8V. Figure 10 shows cell charge distribution of fully processed 64Mb 1T1C FRAM. Wide sensing window of 300 mV was obtained from our 64Mb 1T1C FRAM. Figure 11 shows cell charge characteristics of 64Mb FRAM after baking at accelerated 150°C temperature stress. After 100 hours' bake, 250 mV of sensing window was remained, the value of which is enough for safe sensing of the device. Thus, it can be said that our 64Mb 1T1C FRAM is highly reliable and is expected to guarantee 10 years of retention at 85°C.

## 3. Conclusions

64Mb 1T1C FRAM at 180 nm technology node was successfully demonstrated by newly introducing advanced capacitor stack deposition technology and optimized capacitor etching technologies. Sensing window of 64Mb FRAM was evaluated as 300mV at 1.8V.

## References


[1] Kinam Kim et al., Integ. Ferroelectrics,.p97, v.61 (2004)
[2] S.Y. Lee and Kinam Kim, IEDM Tech. Dig.,p547 (2002)
[3] H.J. Joo et al., Symposium on VLSI Technology., p148 (2004)
[4] Y.M.Kang et al,. Sympo. on VLSI Tech. Dig.,p102 (2005)


Table 1. Process & device feature for 64Mb FRAM.

| Process/Device Features | |
|---|---|
| Design Rule | 0.18μm |
| Cell Size | 0.48μm² |
| Cap. Size | 0.28μm² |
| Cap. Stack | Ir/SrRuO₃/ PZT_70nm/Ir/TiAlN |
| Interconnection | W Plug |
| Metallization | 3 Level Metal (W, Al1, Al2) |
| Voltage | 1.8~3.3V |
| Access Time<br>Cycle Time | 80ns<br>100ns |
| Operation &<br>Standby Current | <5mA<br><20μA |

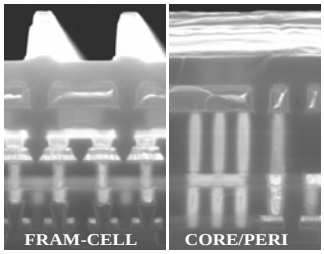


Fig 1. Cross sectional SEM view of unit cell of 64Mb 1T1C FRAM.

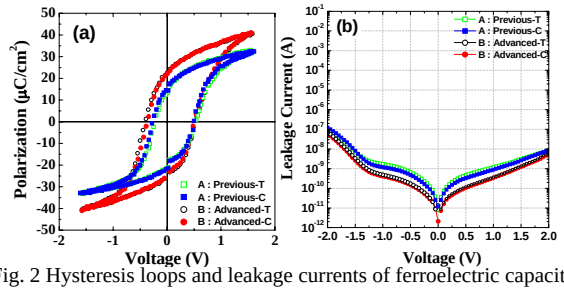


Fig. 2 Hysteresis loops and leakage currents of ferroelectric capacitors with different PZT deposition conditions.

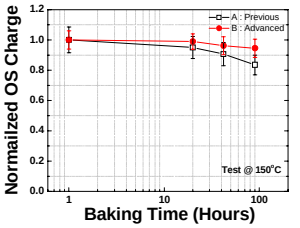


Fig.3. Retention properties of different PZT deposition condition.

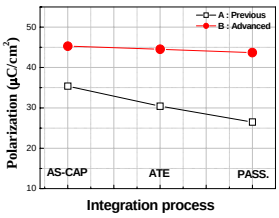


Fig. 4 Degradation of different deposition condition.

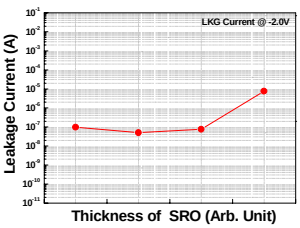


Fig. 5 Leakage current with various thickness of SRO.

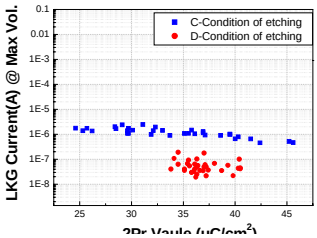


Fig. 6 Leakage currents and 2Pr values for capacitor etch conditions.

Table 2. Capacitor etching condition.

| Cap Etching Condition | C | D |
|---|---|---|
| Mask Etching Plasma | ICP | RIE |
| Electrode Etching Temp. | > 200℃ | < 100℃ |
| Cap Etching Slope | 74° | 72° |

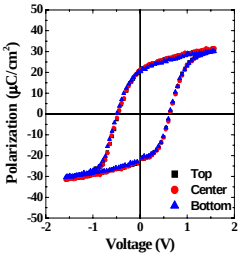


Fig. 7 Hysteresis curves of the capacitor after full-integration.

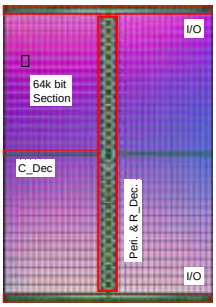


Fig. 8 Optical micrograph of 0.48μm² COB cell 1T1C 64Mb FRAM.

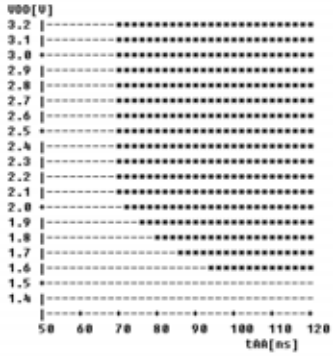


Fig. 9 tAA-VDD Shmoo plot of 64Mb FRAM.

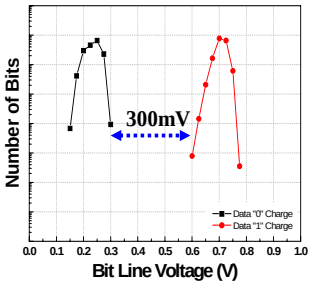


Fig. 10 Charge distribution of fully integrated 64Mb 1T1C FRAM.

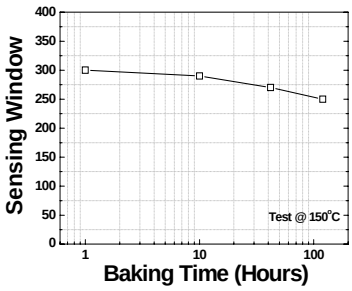


Fig. 11 Sensing Window after accelerating test(150C, 100h bake).