Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 130-131

F-2-1 (Invited)

Overview and Future Challenges eDRAM Technologies

H.sugimura, T.Wake, K.Inoue, M.Hamada, H.Shirai, S.Arai, M.Takeuchi, T.Sakoh, M.Sakao and T.Tanigawa
Advanced Device Development Division, NEC Electronics Corporation
1120 Shimokuzawa, Sagamihara, Kanagawa 229-1198, JAPAN
E-mail:h.sugimura@necel.com

Abstract

This paper presents stacked-capacitor type eDRAM (embedded DRAM) device technologies enabling high-speed random access and low-power operation. Technology trend from 180nm to 55nm generation and future challenges will be described. We have focused onto wide-band data streaming application field such as servers, networks and graphics. For these applications, full compatibility with pure CMOS is essential as they require leading-edge CMOS performance and scaled-down design-rules. The key solution is low temperature stacked-capacitor formation below the thermal budget limitation of leading-edge CMOS Trs. of each generation.

Technology Roadmap

Figure 1 shows cell size trend from 180nm-55nm generation together with the DRAM cell cross-sectional view.

A.(180nm)Co-salicide formation in DRAM cell area and MIS(Metal-Insulator-Silicon) capacitor

Co-salicide formation in DRAM cell area had been the essential technology for boosting eDRAM cell Tr performance and minimizing embedded DRAM fabrication cost [1]. MIS capacitor, consisting of TiN&poly-silicon/Ta_2O_5/hemispherical grained (HSG) silicon, had achieved good C-V & I-V characteristics in this generation.

B.(150nm) MIM(Metal-Insulator-Metal) capacitor

Since 150nm-node, thermal budget limitation of leading-edge CMOS Trs. had decreased to below 600deg C (Fig.2). However, MIS capacitor formation requires annealing at 800deg C to suppress the depletion in the HSG bottom electrode. MIM capacitor technology was developed to solve this issue, keeping compatibility of logic Trs. performance. MIM capacitor, consisting of W-TiN/Ta_2O_5/TiN, can be formed below 500deg C [2]. MIM capacitor also achieved excellent capacitance characteristic with no dependence on applied voltage, as well as well-suppressed leakage current.

C.(130nm)FMD(Full-Metal-DRAM) technology

FMD technology, featuring that major components of DRAM cell are formed of metallic material, drastically reduced parasitic resistances [3]. Cell Trs. SD silicidation and W-plug metal capacitor contacts or bit line contacts have achieved 1/1000 resistance reduction compared with conventional cell technology. From 130nm-node, cell structure has been changed to COB(Capacitor Over Bitline) from CUB(Capacitor Under Bitline) for ensuring cell capacitance in spite of cell size reduction. And wiring metal material has been changed to copper from aluminum. Logic CMOS performance improvement by scaling and eDRAM cell parasitic resistance reduction by FMD enable over 450MHz random access operation @1.2V.

D.(90nm)MIM2 introducing ALD(Atomic-Layer-Deposition) ZrO_2 dielectric

With reduction of cell size, it's hard to keep sufficient cell capacitance using Ta_2O_5 dielectric even for COB structure because of leakage issue. At Teq(equivalent oxide thickness) = 1.5nm, leakage current @100deg C exceeds our criteria. Therefore, we have developed new MIM dielectric material with which leakage current characteristic has very small dependence on temperature. Several high-k materials were investigated, such as HfO_2 or Al_2O_3. Finally, we have chosen ALD ZrO_2 dielectric. Figure 3 shows excellent leakage current characteristic of ZrO_2 compared with other high-k materials @125deg C. We named this W-TiN/ZrO_2/TiN structure capacitor MIM2. This MIM2 can be formed below 400deg C so that it dose not affect logic CMOS performance at 90nm-node and beyond. The compatibility of pure logic Trs. is shown in Fig.4.

Future Challenges

A.(55nm) High-k Gate-dielectric Technology

Beyond 55nm-node, as gate oxide thickness is scaled down to improve CMOS performance, Tr. leakage component such as gate leakage or GIDL(Gate-Induced Drain Leakage) becomes an issue especially for low standby-power application. High-k gate-dielectric is developed to solve this conflicting issue, reducing leakage and scaling-down gate oxide simultaneously. This high-k gate dielectric technology exploiting work function modulation, can achieve appropriate Vth with low channel dopant concentration [4]. Low channel doping realizes several desirable characteristics, such as higher mobility, GIDL reduction, device variability reduction, and gamma coefficient reduction. DRAM Cell Trs. are also well-benefited from these high-k gate Tr. characteristics. For example, figure 5 compares Vth-Vsub of cell Tr. with and without high-k, showing that gamma coefficient is reduced by using high-k Tr.

B.(45nm and beyond) Technical Issues

Scaled-down stacked type eDRAM has several issues, such as limitation of thermal budget, increase of contact resistance and capacitance reduction. MIM(MIM2) and FMD Technologies have solved these issues. We believe these solutions are extendible to 45nm-node. For 32nm-node and beyond, new materials or new structures may be required.

Acknowledgment

The authors appreciate S. Kishi, Y. Yamagata and T. Kuwata for their advices and encouragements. We also thank T. Kitamura and Y. Aoki for their technical support.

References
[1]M. Hamada et al., IEDM Tech. Dig., p45-48, 1999
[2]M. Takeuchi et al., Symp. on VLSI Tech., p29-30, 2001
[3]S. Arai et al., IEDM Tech. Dig., p403-406, 2001
[4]Y. Yasuda et al., IEDM Tech. Dig., p73-76, 2005

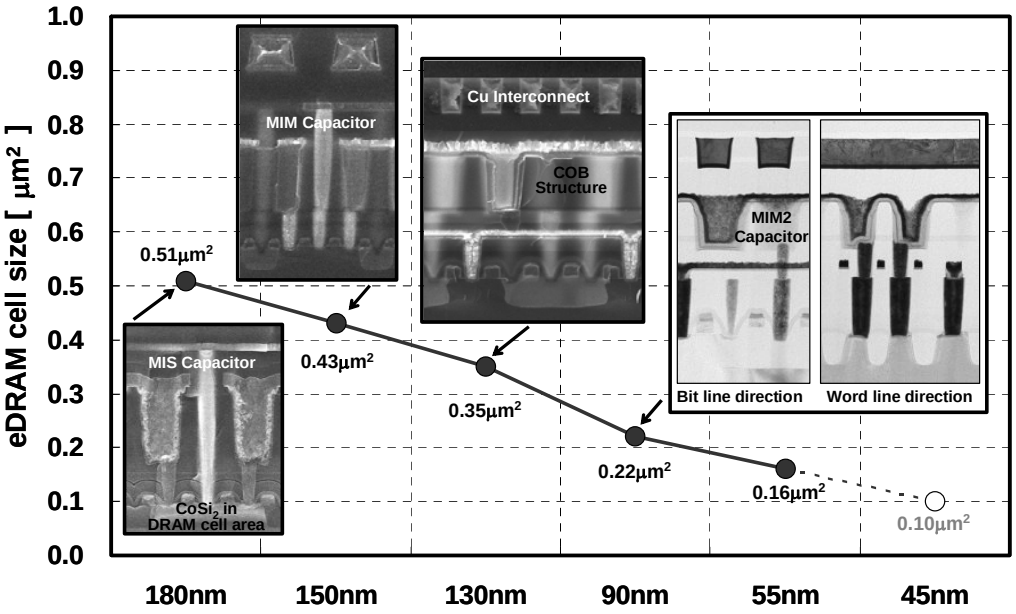

Fig.1 eDRAM Road Map

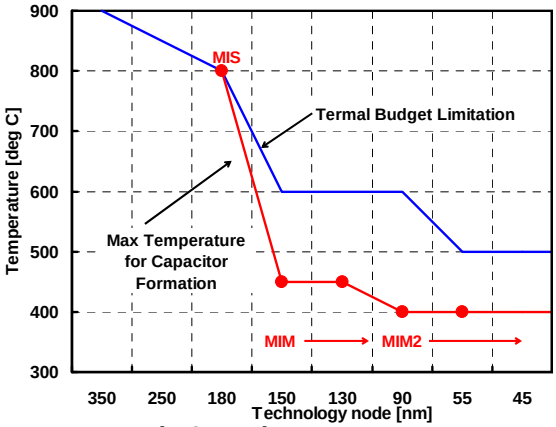

Fig.2 Maximum Temperature for Capacitor Formation

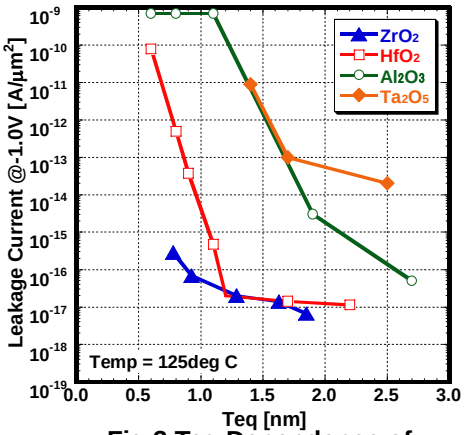

Fig.3 Teq Dependence of Leakage Current @ 125 deg C

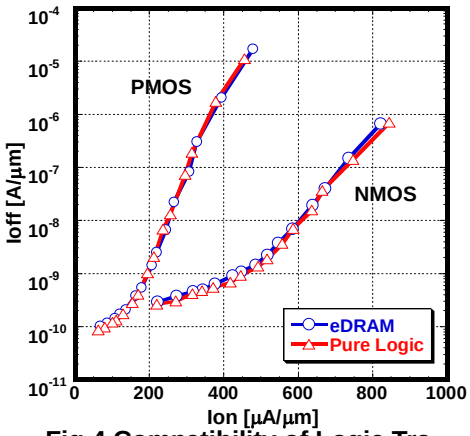

Fig.4 Compatibility of Logic Trs. @ 90nm-node

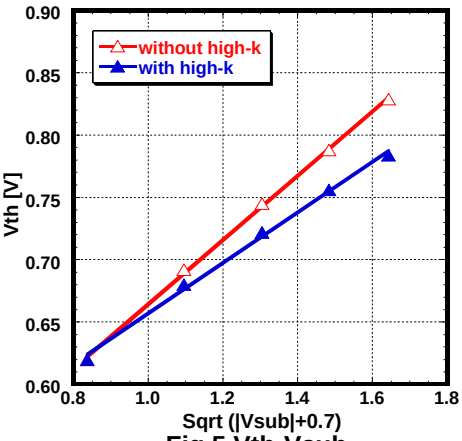

Fig.5 Vth-Vsub of 55nm-node