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Robust and Cost-Effective MIS-Al_2O_3/SiON Double-Layered Capacitor Technology for Sub-90 nm DRAMs

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1. Introduction

Increasing area of DRAM capacitor places strict demands on robustness and cost effectiveness. An importance of robustness comes from requirements to suppress characteristic fluctuation enhanced by the area of capacitor larger than die size. Although Metal-Insulator -Metal is thought to be introduced for its thinner effective oxide thickness (EOT) for sub-90 nm, some breakthroughs are still necessary due to its high density of defects. On the other hand, Meta-Insulator-Semiconductor (MIS) structure has already been verified in volume production. Thus we made a study on the MIS-Al_2O_3 to extend the technology to less than 90 nm. A further study gives us two key processes shown in Table. 1. The first one is atomic layer deposition (ALD) of Al_2O_3 with H_2O for oxidant and post-deposition anneal (PDA) in O_3. This process has a good step coverage [1], and therefore high throughput, which leads to cost effectiveness. The other is silicon-oxynitride (SiON) interface with optimized process [2]. Application of SiON provides low leakage-current variation, which leads to robustness. The fabricated capacitor shows EOT of less than 3 nm with sufficiently low leakage current as shown in Fig. 1, and lifetime of far beyond 10 years. We believe this technology is compatible with sub-90 nm DRAM.

2. Experiments

We fabricated an MIS-Al_2O_3/SiON planer capacitor. P-doped poly-silicon surface was nitrided by NH_3 annealing. Next, we oxidized Si_3N_4 by NO annealing. Then, H_2O-based Al_2O_3 was deposited by ALD. After that, we applied PDA in O_3. Last, TiN was deposited for an upper electrode. We measured a capacitance, leakage current, and TDDB to analyze capacitor characteristics.

3. Results and Discussion

A. Cost-effective processes of H_2O-based Al_2O_3 and O_3-PDA

We chose optimal oxidant for cost effective ALD of Al_2O_3. The throughput of ALD-Al_2O_3 depends on an adhesiveness of oxidant. Since the sticking coefficient of H_2O is much larger than that of O_3, H_2O is suitable oxidant from a viewpoint of throughput.

However, it is widely known that as-deposited H_2O -based Al_2O_3 shows unacceptable leakage current [3]. To overcome the problem, we used O_3 at low temperature (430ºC). Since diffusion of O_3 in Al_2O_3 is slower than that of O_2 at high temperature, it seems possible to oxidize only Al_2O_3. Then we compared characteristics of an MIS-Al_2O_3 capacitors annealed in O_3 at 430ºC with those annealed in O_2 at 750ºC. As shown in Fig. 2, H_2O-based Al_2O_3 with O_3 PDA shows thinner EOT than that with O_2 PDA. Furthermore, for O_3 PDA of 3 min, the increase of EOT from the as-deposited sample was less than 0.2 nm, and this means that the oxidation of underlying layer was very small.

The critical voltage at the leakage current of 1 μA/cm^2 is significantly enhanced by the O_3 PDA (Fig. 2). To clarify its mechanism, we estimated the barrier height (E_{bh}) by using the method of Itokawa [4], for as-deposited Al_2O_3 and the O_3-annealed one. First, we measured the band gap (E_g) (see Fig. 3) and the valence band offset (E_v) (Fig. 4). Second, assuming

$$E_{bh}=E_g-E_v, \quad (1)$$

we calculated the barrier height; see Fig. 5. As is shown in Table 2, the O_3 anneal increased E_{bh} by 1.0 eV. This is the mechanism of the increase of the critical voltage.

B. Robustness-enhancing interface of SiON

We improved robustness such as leakage current variation and Weibull slope by using SiON interlayer between Al_2O_3 and poly-Si. The SiON is formed by thermal nitridation and weak oxidation. It is obvious that excessive oxidation will make low permittivity SiON, which leads to increase in EOT. Then we searched for the oxidation process with sufficient controllability. We selected NO for annealing gas, because its oxidation degree is weaker than that of N_2O or O_2, so that it can be controlled in required range by adjusting annealing temperature.

We applied the NO annealing process to fabricate test capacitors and tested capacitance, leakage current, and time dependent dielectric breakdown (TDDB) at 90 ºC. An optimized SiON ($\varepsilon_r \sim 5.5$ - 6.0) is supposed to have less defects than strongly oxidized SiON ($\varepsilon_r < 5.5$). Actually, as shown in Fig. 6, by applying the optimized SiON, the leakage current was completely limited below 1×10^{-8} A/cm^2 with EOT less than 3.0 nm. (This value was converted from minimum capacitance between -1 V and 1 V.) On the other hand, by using strongly oxidized SiON, the leakage current showed large variation due to higher defect density, leading to a critical degradation of reliability. Accordingly, the Weibull slope was improved from 1.1 to 2.0 by changing from low permittivity SiON to optimized one.

Using the TDDB data, we estimated the chip-level lifetime of the optimized MIS-Al_2O_3/SiON capacitor (see Fig. 7). The lifetime was defined as the threshold time of a defective fraction exceeding 100 ppm. The area of capacitor and stress voltages are extrapolated to the total area of 1-Gb DRAM and to operating voltage of 1 V, respectively. The estimated lifetime was far beyond 10 years. We believe this process makes it possible to apply a robust MIS structure to 65 nm when Al_2O_3/HfO_2 dielectric is used.

4. Conclusion

We developed deposition process and PDA of ALD-Al_2O_3, and interfacial technique of SiON, to fabricate cost effective and robust MIS capacitor. We chose H_2O-based ALD-Al_2O_3 to realize high throughput, and PDA in O_3 at low temperature to reduce the leakage current. We also used optimized SiON interlayer to suppress

leakage current variation. By using these techniques, we successfully fabricated an MIS-Al_2O_3/SiON capacitor with an EOT less than 3 nm and a lifetime of more than 10 years. These technologies provide robust and cost effective capacitor for sub-90 nm DRAM.

Acknowledgement

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References

[1] G. Prechtl *et al.*, *IEDM Tech. Dig.*, (2003) p.245.
[2] O. Tonomura *et al.*, *SSDM*, (2003) p.244.
[3] Y. K. Kim *et al.*, *IEDM Tech. Dig.*, (2000) p.369.
[4] H. Itokawa *et al.*, *SSDM*, (1999) p.152.
[5] I-S. Park *et al.*, *VLSI Tech. Dig.*, (2000) p.42.
[6] ITRS 2005

Table.1 Technologies of MIS-Al_2O_3/SiON capacitor for DRAMs

	Conventional work [5]	This work	
Dielectrics	O_3-based Al_2O_3	H_2O-based Al_2O_3 + O_3 PDA	(Application of H_2O for oxidant permit both speedy and high-step -coverage deposition, which leads to **Cost effectiveness.**)
Interface	SiO_2 (ε_r~3.9)	SiON (ε_r~5.5-6.0)	(Application of lower-defect-density interface of SiON realize less characteristic fluctuation, which leads to **Robustness.**)

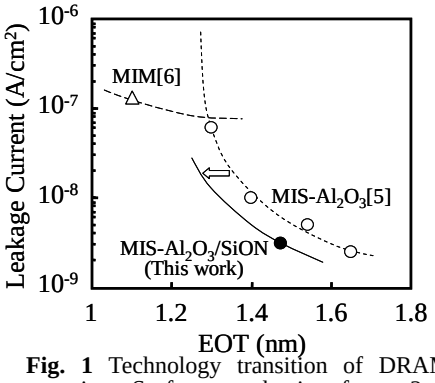


Fig. 1 Technology transition of DRAM capacitor. Surface roughening factor 2 is used for effective EOTs in the case of MIS.

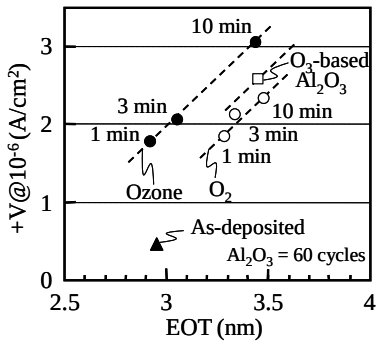


Fig. 2 Capacitor characteristics with PDA in oxidizing atmosphere. O_3 anneal reduces leakage current with slight increase in EOT.

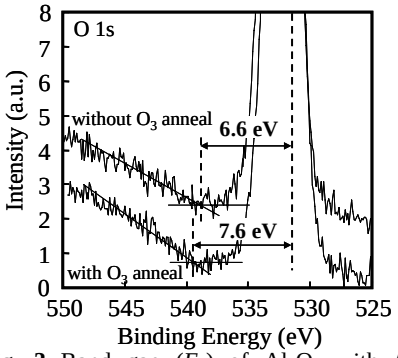


Fig. 3 Band gap (E_g) of Al_2O_3 with / without O_3 anneal extracted by O*1s* peak measured by XPS.

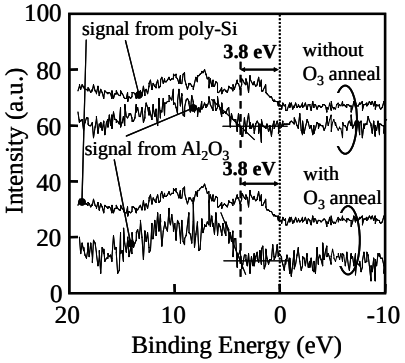


Fig. 4 Evaluation of valence band offset (E_v) between Al_2O_3 and poly-Si with / without O_3 anneal from valence band spectra measured by XPS.

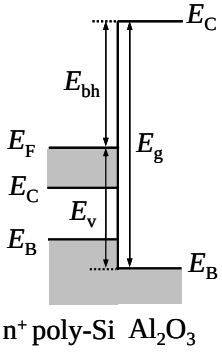
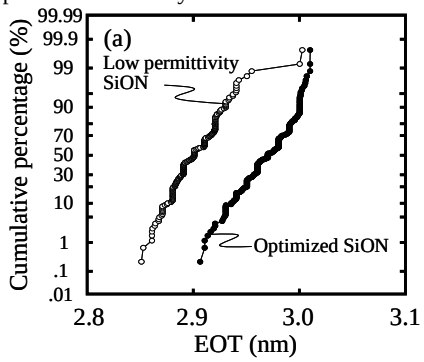


Fig. 5 Assumption of relation among barrier height (E_{bh}), band gap (E_g) and valence band offset (E_v) for Al_2O_3/poly-Si.

Table. 2 Barrier height (E_{bh}) calculated with band gap and valence band offset by using an assumption shown in Fig.5.

	E_g	E_v	E_{bh}
without O_3 anneal	6.6	3.8	2.8
with O_3 anneal	7.6	3.8	3.8

(eV)



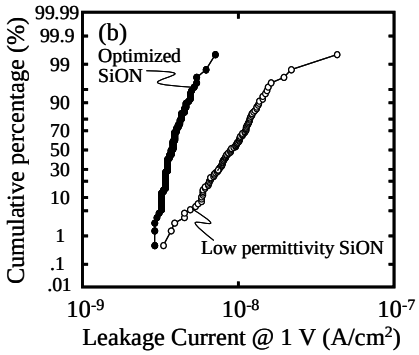


Fig. 6 Cumulative distribution of (a) EOT and (b) leakage current of MIS-Al_2O_3/SiON with optimized SiON and low permittivity one. Optimized SiON with permittivity of 5.5-6.0 decreased leakage current with slight increase in EOT.

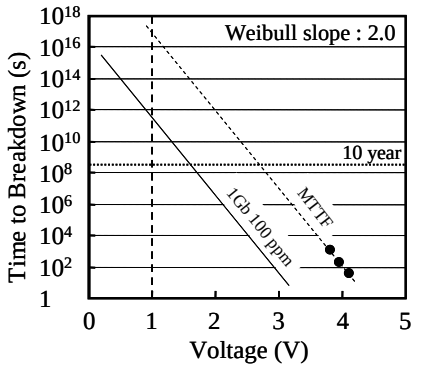


Fig. 7 Lifetime extrapolated to the operation voltage of 1 V calculated by using mean time to failure and Weibull slope. The fabricated MIS-Al_2O_3/SiON capacitor shows lifetime far beyond 10 years.