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Diffusion Barrier Characteristics of TiSix/TiN for Tungsten Dual Poly Gate in DRAM

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INTRODUCTION

Due to the demand of high density and high speed dynamic random access memory (DRAM), gate electrode with a low specific resistance is strongly required to reduce RC delay. For this reason, tungsten polymetal gate could be a good candidate to replace the conventional tungsten polycide gate. However, there are some controversies in choosing an adequate diffusion barrier metal which is crucial for preventing abnormal silicidation between tungsten and poly-Si during post thermal process. In interconnection process, TiN processes are well known to give good characteristics as a diffusion barrier for Al or Cu-based multilevel metallization [1]. Also TiSix/TiN bilayer was reported to show low contact resistance, low stress and flat interface. Recently, some reports have been made for the application of Ti insertion to W poly gate process with a low Rc value [2, 3]. But detailed analysis about interfacial characteristics for the TiSix/TiN diffusion barrier has not been made. Also, dual poly gate processes are strongly required to suppress the short channel effect caused by shortened gate channel length. In p-channel MOSFET, boron penetration into gate oxide could degrade device performance significantly due to flat band voltage shift and increase of interface charge trap density [4, 5]. Increasing the dielectric constant of the top surface gate oxide by plasma nitridation could block boron penetration into gate oxide effectively. However, owing to the high diffusivity of boron in tungsten, it is inevitable for boron to out-diffuse into upper W electrode during thermal processes, which results in severe poly depletion effect. Therefore, inserted barrier metal should also be act as a good barrier which prevents boron from out diffusing into W layer. In this paper, diffusion barrier characteristics of W dual poly gate which involves Ti or TiN were investigated. Barrier characteristic issues relating Ti or TiN inserted gate stack, including gate contact resistance are addressed. The effects of improving p+ poly depletion effect will be shown for W/WN/(TiN)/(Ti)/p+ poly-Si gate stack in detail.

EXPERIMENTAL

To study diffusion barrier characteristics for W dual poly gate stack, various barrier metals ((Ti)/TiN/(WN)) were prepared by sputtering method. After deposition of W poly gate stack, post thermal treatment was applied for all stacks. X-ray Photoelectron Spectroscopy (XPS) was conducted for barrier metal characterization. To investigate the barrier effect of blocking dopant out diffusion, Secondly Ion Mass Spectroscopy (SIMS) was performed. To compare Poly Depletion Ratio (PDR) dependent on diffusion barrier metal, Capacitance-Voltage (CV) was measured on 100X100 um^2 NMOS capacitors. Thickness of each layer of gate stack is summarized in Table 1. Transmission Electron Microscope (TEM) and Electron Energy Loss Spectroscopy (EELS) were conducted for the analysis of interfacial properties. Diffusion barrier dependent gate contact Rc values between W and poly-Si were measured with 4-probes Kelvin method.

RESULTS AND DISCUSSION

To investigate the effect of diffusion barrier of (Ti)/TiN on preventing silicidation between tungsten and poly-Si, we conducted XPS analysis for TiN/(Ti)/Si stacks without additional diffusion barrier. All stacks were annealed at 850°C for 2' in N_2 ambient. In TiN/Ti/Si stacks, both Si-N and Si-Si peaks are observed for various glancing angles, whereas we can not see the Si-N peak after sputtering top surface of TiN layer as shown in Fig. 1. Therefore, Si atoms were considered to be diffused into the top surface during annealing. Fig. 2 shows that all stacks which have different thicknesses of TiN layer show the same intensity of Si-N peak. Accordingly, we can conclude that additional diffusion barrier such as WN is needed to suppress the diffusion of Si into W for Ti/TiN barrier. On the other hand, Si-N peak is still observed for TiN/Si stack after the sputtering as shown in Fig. 3. Dielectric Si-N layer, which could increase gate contact Rc value drastically, is considered to be formed between TiN and Si layer. W/WN layer was deposited on the various diffusion barriers, followed by post thermal anneal process. Fig. 4 shows the results of measured Si2p spectrum after removing top W layer. W/WN/TiN/Si stack shows the same level of Si-N for W/WN/Si stack, but the stacks with Ti layer on the Si do not show Si-N peak. Cross sectional TEM analysis was conducted for the various W/WN/TiN/(Ti)/Si gate stacks. Fig. 5 shows that all stacks show good interfacial properties after post thermal treatment. Fig. 6 and 7 shows SIMS profiles for phosphorous and boron remaining in poly-Si respectively. We can see that all stacks do not show any difference of remaining phosphorous profile in poly Si as shown in Fig. 6. However each gate stack shows different boron concentration near the bottom of gate poly-Si as shown in Fig. 7. TiN/WN barrier exhibits the most amount of remaining boron concentration which shows good function of blocking boron from out diffusing into W due to the existence of dielectric Si-N inter layer. On the other hand, Ti/TiN/WN barrier shows the least amount of remaining boron. To compare p+ PDR electrically, CV characteristics were measured on the fabricated MOS capacitors. We varied the type gate poly-Si (n+ and p+) of the n-channel MOS capacitors. Measurement was performed in negative bias (accumulation mode to channel) to extract the PDR (= Cap. for p+ poly / Cap. for n+ poly). Using this scheme, we could easily measure PDR without fabricating MOSFET. Fig. 8 shows the measured CV characteristics for Ti/WN barrier. Measured PDR for each diffusion barrier is shown in Fig. 9. P+ PDR is degraded for thin CET due to the increase of electric field in gate oxide. Fig. 10 shows that measured PDR for each diffusion barrier has the same trend of SIMS. For W/WN/Ti/poly Si stacks, inserted Ti layer is considered to transform into TiSix/TiN bilayer because of the interaction with dissolved nitrogen in WN (top) and poly Si (bottom) during thermal process. EELS analysis was performed to investigate interfacial properties of for W/WN/Ti/poly-Si stack in detail, which is shown in Fig. 11. For the case of Ti (60Å), we can see the TiSix and TiN formation during post thermal process. We could not discriminate TiSix layer formed for Ti (30Å) case, which is considered to be too thin to observe. The thickness of TiSix for Ti/WN barrier metal is considered to be smaller than that of Ti/TiN/WN barrier metal as shown in Fig. 12. Accordingly, the amount of boron diffused into TiSix layer must be smaller for Ti/WN barrier than Ti/TiN/WN barrier, which could results in enhanced p+ PDR which was shown earlier. To compare the gate contact resistance, Kelvin chain Rc was measured for each gate stack (p+ poly gate and n+ poly gate respectively). Ti/(TiN)/WN barrier shows much lower Rc value compared to conventional WN only barrier which is attributed by the non existence of inter dielectric Si-N layer as shown in Fig. 13. Ti/WN barrier shows lower Rc value than that of Ti/TiN/WN barrier.

CONCLUSION

We investigated various diffusion barrier characteristics for tungsten dual poly gate stack in DRAM. Ti/WN diffusion barrier metal exhibits lowest gate contact Rc due to the uniform formation of TiSix on poly-Si. Also top layer of inserted Ti was converted to TiN from the interaction with dissolved nitrogen in WN during post thermal process, which could act as a good barrier preventing boron out diffusion into tungsten layer.

REFERENCES

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Layer	Thickness
W	400Å
WN	50Å
TiN	40Å
Ti	30Å
Poly-Si	800Å

Table 1. Thickness of each layer of gate stack.

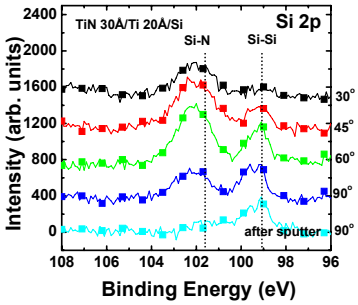

Fig. 1. XPS analysis for TiN/Ti diffusion barrier.

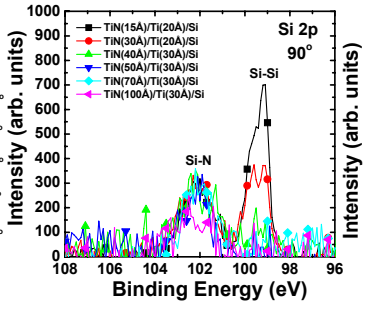

Fig. 2. XPS analysis for TiN/Ti diffusion barrier with various thicknesses.

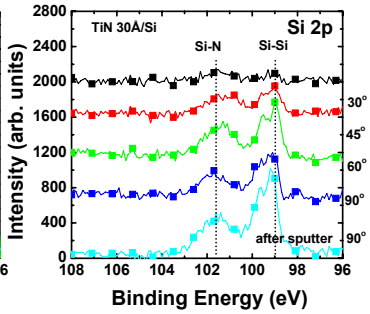

Fig. 3. XPS analysis for TiN diffusion barrier.

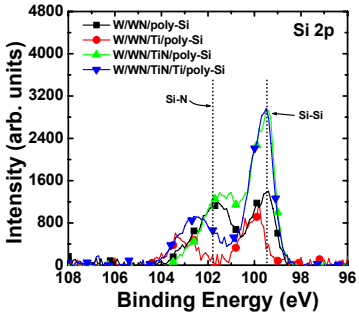

Fig. 4. XPS analysis for various gate stacks.

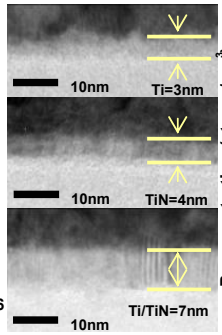

Fig. 5. TEM analysis for gate stacks.

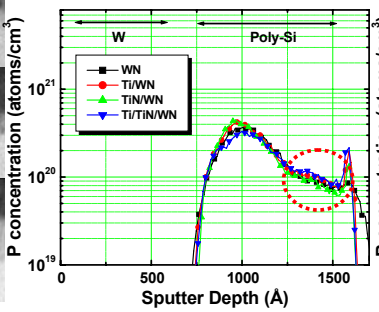

Fig. 6. Phosphorous SIMS profiles for different gate stacks

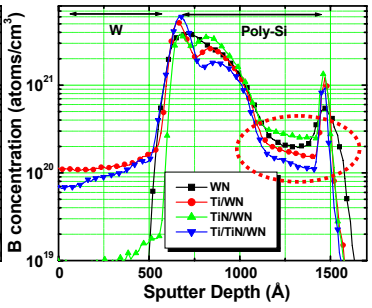

Fig. 7. Boron SIMS profiles for different gate stacks

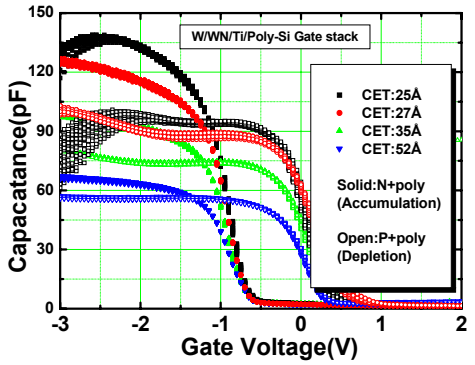

Fig. 8. Result of CV measurement for Ti/WN diffusion barrier.

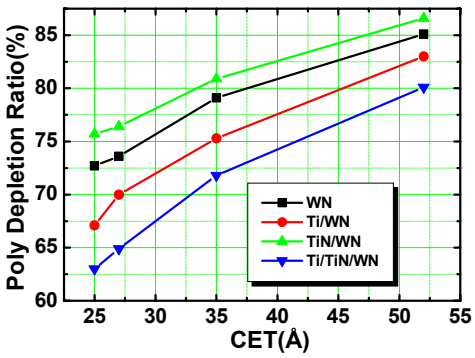

Fig. 9. Poly depletion ratio for different diffusion barriers.

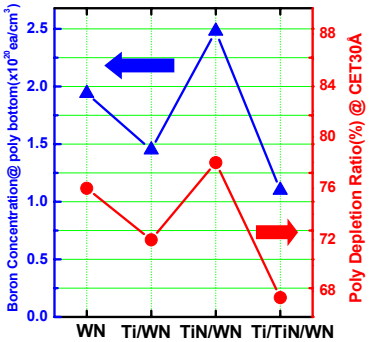

Fig. 10. Comparison between PDR and SIMS for different diffusion barriers.

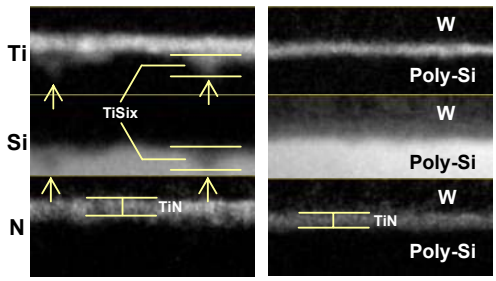

Fig. 11. EELS analysis for W/WN/Ti/Si gate stacks after post thermal treatment. Left (Ti:60Å), Right (Ti:30Å)

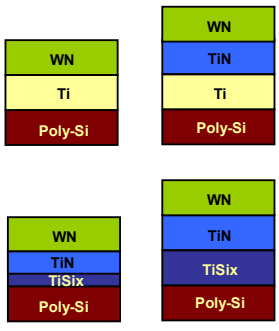

Fig. 12. Schematic cross section for W/WN/Ti/Si and W/WN/TiN/Ti/Si, Top (As depo.), Bottom (After thermal process).

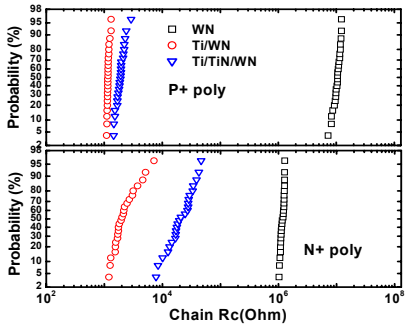

Fig. 13. Kelvin chain Rc for different barrier metals.