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Gate Workfunction Engineering of Bulk FinFETs for Sub-50 nm DRAM Cell Transistors

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1. Introduction

As the DRAM cell size shrinks to sub-50 nm, it becomes critical issue to gain sufficient on-current, low voltage operation, and low off-state leakage current (I_{off}) [1]-[4]. The fabricated FinFETs on the bulk Si wafers is one of the candidates to overcome the above issues. Damascene FinFET structure was proposed with local channel implantation scheme [1]. The cell transistors using n^+ poly gate has a low V_{th}, resulting in high I_{off}. The p^+ poly gate gives high V_{th}, but high I_{off} due to GIDL. Therefore, now it is very difficult to get reasonable DRAM cell operation with n^+ or p^+ poly gate in the sub-50 nm regions.

In this work, we propose a new p^+/n^+ gate FinFETs, and consider device design of the sub-50 nm cell transistors in terms of GIDL using 3-D device simulator.

2. Device Structure and Simulation

The proposed p^+/n^+ poly gate FinFET is shown schematically in Fig. 1. H_{fin} and W_{fin} stand for the gate height and fin body width, respectively. The gate consists of poly-Si with two different work functions. The L_m and L_s represent main p^+ poly gate length and subsidiary n^+ poly gate length, respectively. The x_j is source/drain junction depth defined as a depth from the top of the fin body. In this work, the H_{fin} and the x_j are fixed at 50 nm and 60 nm, respectively. Gate oxide thickness (T_{ox}) is fixed at 3 nm. The uniform body doping is 1×10^{17} cm^{-3} and a local doping which is characterized by Gaussian profile with a peak doping of 3×10^{18} cm^{-3} is adopted just under the LDD x_j to suppress punchthrough. In 3-D device simulation, we adopted band-to-band (BTB) tunneling model to see drain leakage current including GIDL component.

3. Results and Discussion

Fig. 2 shows the 2-D I_D-V_{GS} characteristics as parameters of W_{fin} and LDD concentration. To exclude I_{off} change due to DIBL, we used n^+ poly gate devices with an L_g of 100 nm. Those devices have a peak body doping (3×10^{18} cm^{-3}) at the center between source and drain. GIDL current increases as the LDD doping increases. With decreasing W_{fin}, GIDL current decreases due to the decrease of electric field in the LDD region overlapped by the gate. Fig. 3 shows I_D-V_{GS} characteristics with the L_s at fixed L_g of 50 nm and W_{fin} of 20 nm. The n^+ only or p^+ only gate device gives larger I_{off} than 1 fA. By controlling L_s, we can obtain a minimum I_{off} by ~10^{-17} A at V_{GS}=0 V and V_{DS}=1.5 V. The extracted I_{off}'s and V_{th}'s are shown in Fig. 4. As the L_s increases from 0 nm to ~25 nm, the V_{th} decreases very slowly and then decreases significantly. Optimum L_s is ~15 nm at given L_g of 50 nm and W_{fin} of 20 nm. It is needed to check internal physics to understand I_{off} variation. Fig. 5 shows the surface potential profile in the channel region along the cut line located near the top silicon region of fin body. We can observe different slope in the L_s region for the p^+/n^+ gate device. The area under the p^+ poly gate of the p^+/n^+ gate FinFET is essentially screened from the drain-potential variation [5]. Fig. 6 shows the electric field along the Si channel near the top silicon surface. Compared to p^+ gate device, p^+/n^+ gate gives lower peak electric field, which leads to lower GIDL. Fig. 7 shows the electric field profiles obtained at the same position as that in Fig. 6. The L_s changes from 5 nm to 15 nm. As the L_s increases, the peak electric field inside channel decreases, and the electric field near drain junction decreases. Fig. 8 shows I_{on}'s of the p^+/n^+ gate FinFETs with L_s/L_g (0.1, 0.2, and 0.3) and W_{fin} as a parameter of L_g at V_{DS}= V_{GS}= 1.5V. With increasing L_s/L_g, the I_{on} increases due to V_{th} reduction. The I_{on} also increases as the W_{fin} increases because of DIBL increase. The maximum I_{on} is about 35 μA when based on the I_{off} requirement (< 1 fA) shown in Figs. 9 to 11. The I_{off}'s by changing W_{fin} and L_s at a fixed L_g are shown in Figs. 9 to 11, where solid symbols meet the I_{off} requirement. To guarantee I_{off} less than 1 fA, the L_s at L_g=30 nm should be less than ~6 nm for a given W_{fin} of 15 nm. 40 nm devices require W_{fin} less than 20 nm for given L_s of 4 nm to 12 nm to meet the requirement. The devices with an L_g of 50 nm show I_{off}'s less than 1 fA for the L_s of 5 nm to 15 nm at given W_{fin} of 10 nm to 30 nm. If the L_s goes to 0 or 50 nm, then the I_{off} becomes larger than 1 fA. In Table 1, shown are DIBL and SS characteristics of the proposed devices. The 30 nm devices need the W_{fin} less than ~15 nm to keep the DIBL less than 100 mV/V. For 40 nm devices, the W_{fin} needs to be less than ~20 nm to keep the DIBL less than 100 mV/V.

4. Conclusion

We have proposed a new p^+/n^+ gate FinFET and considered device design for sub-50 nm DRAM cell transistors. Based on the I_{off} requirement (< 1 fA), we suggested reasonable n^+ subsidiary gate length and fin body width for the cells with L_g's of 30, 40, and 50 nm.

Acknowledgements

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References

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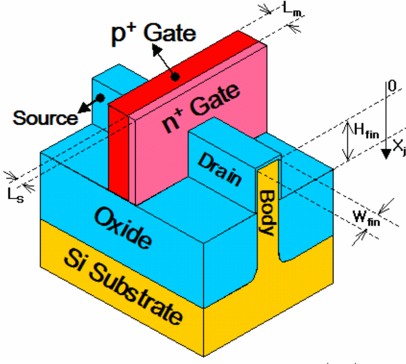

Fig. 1. 3-D schematic view of p^+/n^+ gate FinFET. H_{fin} and W_{fin} stand for the fin height and fin body width, respectively. Here, L_g is given by L_m+L_s, where L_s is the length of n^+ poly gate.

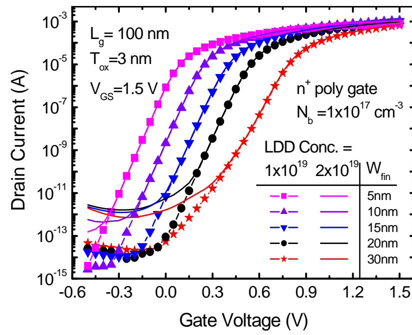

Fig. 2. 2-D I_D-V_{GS} characteristics as parameters of W_{fin} and LDD doping. The data for LDD concentrations of 1×10^{19} cm^{-3} and 2×10^{19} cm^{-3} are represented by symbols and simple lines, respectively.

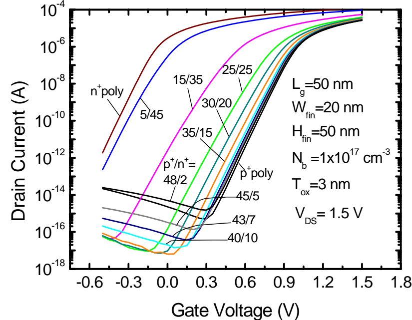

Fig. 3. I_D-V_{GS} characteristics by changing the L_s at a fixed L_g of 50 nm. Here the W_{fin} is fixed at 20 nm.

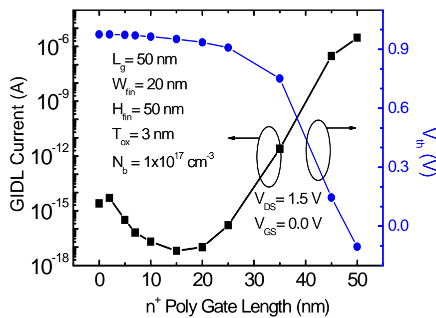

Fig. 4. I_{off} and V_{th} versus the L_s at a fixed L_g of 50 nm. I_{off} values were captured at V_{GS} of 0 V and V_{DS} of 1.5 V.

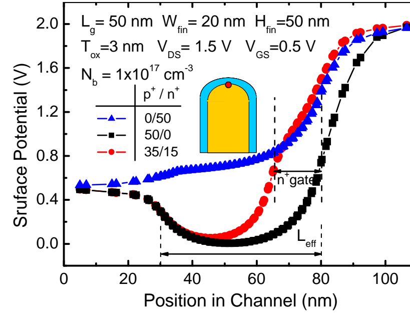

Fig. 5. Surface-potential profiles of n^+-poly, p^+-poly and p^+/n^+-poly gates at a fixed L_g of 50 nm. The insert shows a cutting point near the silicon interface on the cross-sectional view of the fin body.

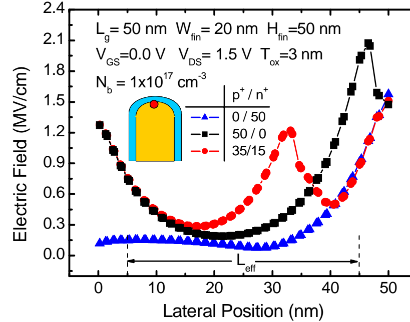

Fig. 6. Electric-field profiles along the channel at the silicon top region of fin body for different L_s's.

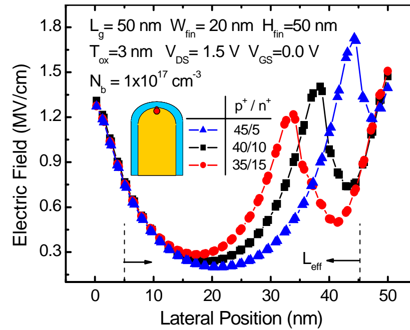

Fig. 7. Electric-field profiles along the channel at the silicon top region of fin body. The L_m and L_s are changed at a fixed L_g of 50 nm. Given V_{GS} and V_{DS} are 0 V and 1.5 V, respectively.

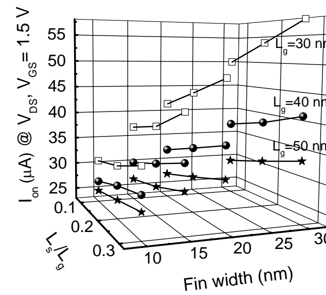

Fig. 8. I_{on} characteristics with L_s/L_g and W_{fin} as a parameter of L_g. The rectangle, circle and star symbols represent the data for L_g= 30 nm, L_g= 40 nm and L_g= 50 nm, respectively.

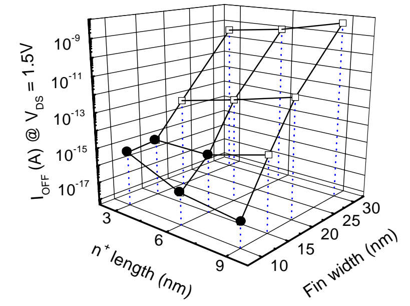

Fig. 9. I_{off} of 30 nm devices with W_{fin} and L_s. The solid symbols represent the I_{off}'s less than ~1 fA.

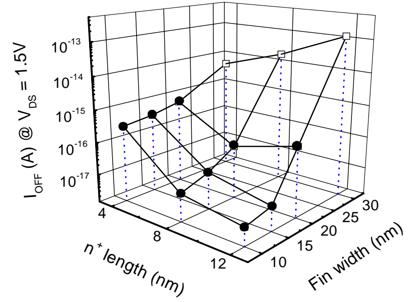

Fig. 10. I_{off} of 40 nm devices with W_{fin} and L_s. The solid symbols represent the I_{off}'s less than ~1 fA.

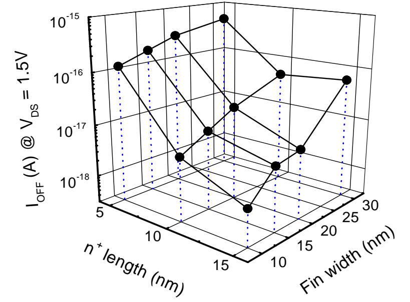

Fig. 11. I_{off} of 50 nm devices with W_{fin} and L_s. The solid symbols represent the I_{off}'s less than ~1 fA.

Table 1
Electrical characteristics of the FinFET with the W_{fin} and L_s

(a) L_g= 30 nm

	DIBL (mV/V)			SS (mV/dec)		
W_{fin} \ L_s	3 nm	6 nm	9 nm	3 nm	6 nm	9 nm
10 nm	59.93	63.1	66.69	69.05	69.2	69.78
15 nm	112.4	117.2	118.6	77.41	77.6	78
20 nm	181.4	187.6	188.3	88.47	89.99	93.63
30 nm	349.6	357.24	363.8	129.1	134.5	149.5

(b) L_g= 40 nm

	DIBL (mV/V)			SS (mV/dec)		
W_{fin} \ L_s	4 nm	8 nm	12 nm	4 nm	8 nm	12 nm
10 nm	28.21	31.03	35.24	64.4	64.75	65.06
15 nm	52.96	57.03	62.27	69.39	69.78	71.07
20 nm	84.13	90.34	97.93	76.35	76.82	77.94
30 nm	155.17	168.28	178.62	93.79	95.23	96.93