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# Intrinsic Delay of Nanoscale MOSFETs under Ballistic Transport

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## I. Introduction

Quasi-ballistic carrier transport is one of the technology boosters to enhance drain current in nanoscale MOSFETs [1]. Channel backscattering characteristics are the key to limiting the drain current at the rate which carriers can be thermally injected from the source into the channel, as illustrated in Fig. 1, is formulated as

$$I_{\rm d}/W = Q(0)v_T(1-r)/(1+r) = Q(0)v_{eff} \quad (1)$$

and is valid when $V_{\rm ds} >> k_BT/q$ [2]. The critical parameters are the density of the carriers at the top of the barrier in the source edge, $Q(0)$, the thermal injection velocity, $v_{\rm T}$ theoretically given by [3], and the channel backscattering coefficient $r$ ($0 < r < 1$), which can be determined by $k_BT$ layer thickness $l_0$ and mean-free-path for backscattering $\lambda_0$ [2]. Note that $r = l_0/(\lambda_0 + l_0)$. The $v_{\rm eff}$ represents effective carrier velocity. To determine $Q(0)$, the gate capacitance measured with a large device was integrated over the gate voltage at $V_{\rm ds}$ = 0V [4]. However, lateral channel profiles along the gate length and width direction formed by halo or pocket implants in a small device are completely different from those in a large device [5]. This paper proposes a new procedure for direct measurement of $Q(0)$ in short channel devices and demonstrates the impact of gate scaling on the channel backscattering coefficient in nanoscale MOSFETs with varying physical gate lengths down to 68nm.

## II. Procedure of evaluation

Fig. 2 shows an example of $Q(0)$ determination. For the small device, external capacitance $C_{\rm ext}$ such as overlap and fringing capacitances cannot be neglected, so the area described by the hatched region under the solid curve corresponds to $Q(0)$. Fig. 3 shows the proposed test structure that consists of a charge based capacitance measurement (CBCM) circuit and a pair of path transistors. The CBCM technique has been widely used to measure femto-farad level capacitance [6]. The waveforms of gate input signals, GP, GN and EN are shown in Fig. 4. The channel backscattering coefficient extraction methodology is summarized in three steps as follows; (1) Gate capacitance, $C_{\rm gg}$, is measured from the charging current difference ($\Delta Q_{\rm g}$) with the small increment ($\Delta V$) of $V_{\rm tst}$ and $V_{\rm ref}$ as $C_{\rm gg} = \Delta Q_{\rm g}/\Delta V$ [7], where $Q_{\rm g}$ is the gate charge. (2) A charge, $-C_{\rm gb}\Delta V$, is induced on the target substrate (back) when a charge $C_{\rm gg}\Delta V$ is placed on the target gate electrode through the p-MOSFET MP1. The charging control signal EN is high during $C_{\rm gb}$ measure time period, as illustrated in Fig. 4, so that a measurable charging current is drawn from the target substrate through the current meter (placed at the source of MN4) and to the local ground voltage source. Note that $C_{\rm gg}$ and $C_{\rm gb}$ are measured simultaneously in the short channel devices with sub-femto-farad resolution. (3) Gate-to-channel capacitance, $C_{\rm gc}$, is given by $(C_{\rm gg} - C_{\rm gb} - C_{\rm ext})$. External capacitance, $C_{\rm ext}$, corresponds to $(C_{\rm gg} - C_{\rm gb})$ value at $V_{\rm gs}$ = 0V. The expression for $Q(0)$ as extracted from $C_{\rm gg}$ and $C_{\rm gb}$ becomes

$$Q(0) = qN_{\rm inv} = \int_0^{V_{\rm gs}} (C_{\rm gg} - C_{\rm gb} - C_{\rm ext})dV_{\rm gs}/(L_{\rm eff}W_{\rm eff}) \quad (2)$$

where $N_{\rm inv}$ is inversion charge density, $L_{\rm eff}$ and $W_{\rm eff}$ are effective gate length and width, respectively. $L_{\rm eff}$ is extracted from $C_{\rm gc}$ of some different physical gate length MOSFETs. The channel backscattering coefficient $r$ is extracted from measured $I_{\rm d}$ and $Q(0)$ by using eq.(1).

## III. Results and Discussion

Low standby power (LSTP) MOSFETs employed in this work are fabricated by a hp90-nm technology node process. Capacitance is measured on a small (68nm × 2 $\mu$m) device. Fig. 5 shows the electrical characteristics of the devices demonstrated in this work. Fig. 6 shows $C_{\rm gg}$ and $C_{\rm gb}$ characteristics at $V_{\rm ds}$=0V and 1.2V measured by the proposed test structure. The difference between $C_{\rm gg}$ and $C_{\rm gb}$ at $V_{\rm gs}$=0V corresponds to the total of the gate overlap and fringing capacitance, $C_{\rm ext}$. As the drain voltage increases from 0V to 1.2V, $C_{\rm gb}$ increases under the saturation region because the inversion layer around the drain edge disappears at $V_{\rm ds}$=1.2V, which in turn leads to $C_{\rm gg}$ reduction. Fig. 7 shows extracted inversion charge density $N_{\rm inv}$ at $V_{\rm ds}$=0V and $V_{\rm gs}$=1.2V. The inversion charge density given by $C_{\rm ox}(V_{\rm gs} - V_{\rm th})$, as shown in Fig. 2, is about *2.5* times as large as that extracted by the proposed technique. The almost flat curve indicates that the value of the effective gate length employed for $N_{\rm inv}$ calculation is reasonable. Fig. 8 shows the extracted channel backscattering coefficient $r$ at $V_{\rm ds}$=$V_{\rm gs}$=1.2V. As the gate length shrinks, the backscattering coefficient is reduced, indicating that ballistic transport becomes more evident. Fig. 9 shows extracted ballistic efficiency together with effective carrier velocity $v_{\rm eff}$. In Fig. 10, the $\lambda_0/l_0$ value is plotted versus physical gate length. Extrapolating the straight line in Fig. 10 yields $\lambda_0/l_0$ =8.38 in n-MOSFET and 4.53 in p-MOSFET, when projecting the performance limit of 10nm MOSFETs under supply voltage 1.2V. The $\lambda_0/l_0$ value in turn leads to an on-current approaching 81% of the ballistic limit in n-MOSFET. Fig. 11 shows the extracted intrinsic transistor delay, $C_{\rm gg}V_{\rm dd}/I_{\rm d}$. Intrinsic delay of hp90-nm LSTP MOSFETs found in this work is nearly close to that of ITRS MOSFETs [1]. The corresponding intrinsic delay of 10nm n-MOSFET is 0.11ps, less than that reported in a hp14-nm node process [1] as listed in Table I. The performance of single gate 10nm n-MOSFET estimated from view of ballistic transport meets LSTP hp14-nm node process requirement [1].

## IV. Conclusion

We have proposed a new procedure for evaluating the channel backscattering coefficient on a basis of monitoring gate capacitance and gate-to-substrate capacitance in nanoscale MOSFETs by the new test structure. The new procedure reveals that an advanced n-MOSFET technology with $L_{\rm G}$=10nm operates at no less than 81% of thermal injection velocity. Intrinsic transistor delay, 0.11ps, in single gate 10nm n-MOSFET estimated from view of ballistic transport meets LSTP hp14-nm node process requirement.

### References

[1] The International Technology Roadmap for Semiconductors (ITRS), PIDS, 2005. [2] M. S. Lundstrom et al., *IEEE Electron Dev. Lett.*, vol.18, p.361, 1997. [3] K. Natori, *J. Appl. Phys.*, vol.76, p.4879, 1994. [4] A. Lochtefeld et al., *IEEE Electron Dev. Lett.*, vol.22, p.95, 2001. [5] H. van Meer et al., *IEEE Electron Dev. Lett.*, vol.21, p.133, 2000. [6] J. C. Chen et al., *IEDM Tech. Dig.*, p.69, 1996. [7] T. Okagaki et al., *VLSI Tech. Symp.*, p.120, 2004.

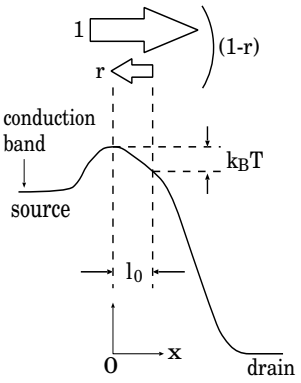


Fig. 1. Schematic diagram of carrier channel backscattering in nanoscale MOSFETs. Carriers injected from the source may be backscattered in $k_BT$ layer.

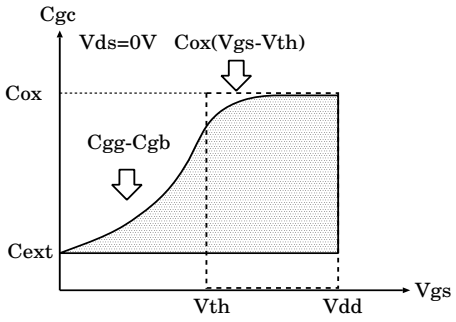


Fig. 2. Schematic diagram of gate-to-channel capacitance vs gate voltage at Vds=0V. Cext represents overlap and fringing capacitance.

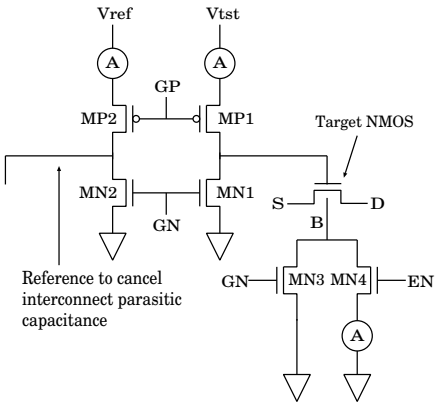


Fig. 3. Proposed test structure for gate-to-channel capacitance characterization.

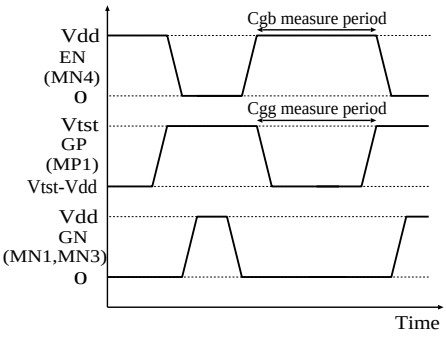


Fig. 4. Schematic gate input waveforms of the proposed circuits.

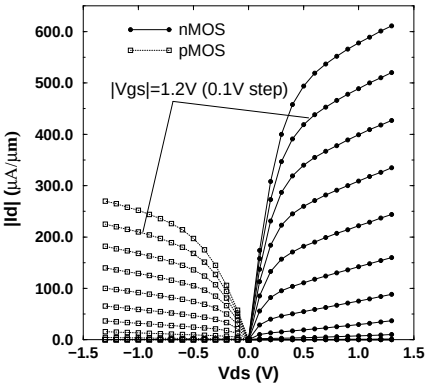


Fig. 5. Id-Vd characteristics of nMOSFET and pMOSFET fabricated by a hp90-nm technology node process.

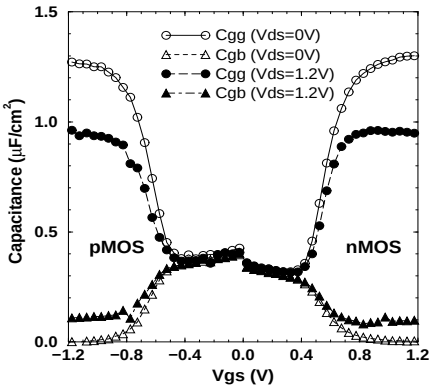


Fig. 6. Cgg and Cgb characteristics at Vds=0V and 1.2V measured by the proposed test structure.

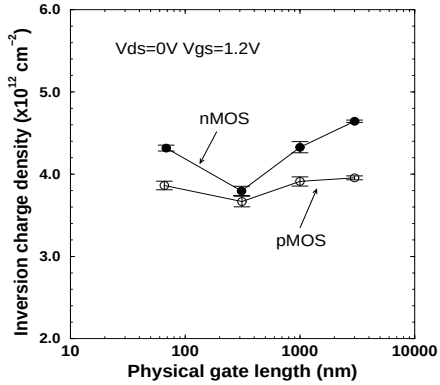


Fig. 7. Extracted inversion charge density Ninv (=Q(0)/q) at Vds=0V and Vgs=1.2V.

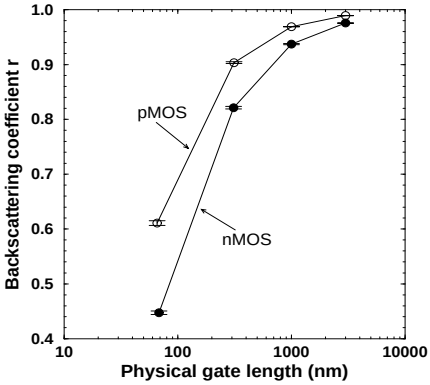


Fig. 8. Extracted channel backscattering coefficient r of MOSFETs at Vds=Vgs=1.2V.

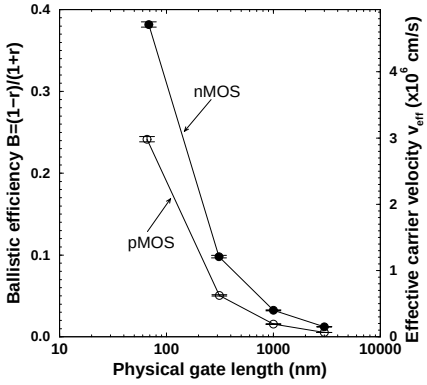


Fig. 9. Extracted ballistic efficiency B=(1-r)/(1+r) and effective carrier velocity $v_{eff}$ = B $v_T$.

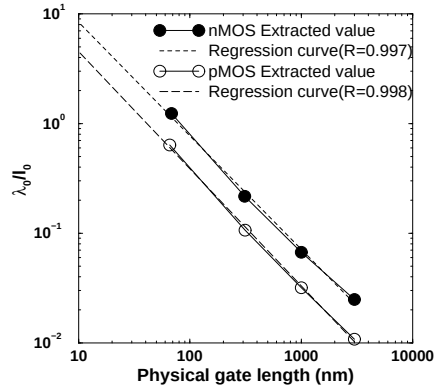


Fig. 10. Extracted $\lambda_0/l_0$ and a regression curve with a correlation coefficient R for projection of 10nm MOSFET performance.

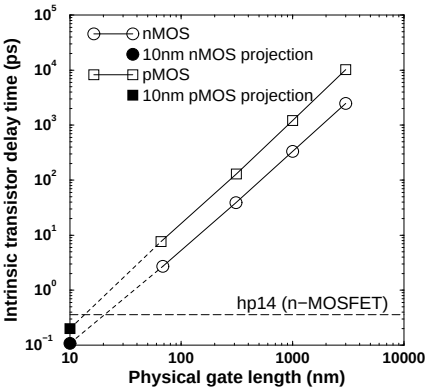


Fig. 11. Extracted intrinsic transistor delay time of n-MOSFET and p-MOSFET.

Table I. Comparison of extracted intrinsic transistor delay time with those from 2005 ITRS.

| Intrinsic Transistor Delay Time (ps) | |
|---|---|
| Present work | |
| · Lg=68nm nMOS | 2.72 |
| · Lg=10nm nMOS projection | 0.11 |
| · Lg=66nm pMOS | 7.66 |
| · Lg=10nm pMOS projection | 0.20 |
| 2005 ITRS hp90-nm Node (Lg=65nm nMOS) | 2.56 |
| 2005 ITRS hp14-nm Node (Lg=10nm DG nMOS) | 0.36 |