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Simulation of Atomic Scale Effects and Fluctuations in Nano-Scale CMOS

Asen Asenov, Andrew R. Brown, Gareth Roy, Craig Alexander and Antonio Martinez

Device Modelling Group, Department of Electronics and Electrical Engineering
The University of Glasgow, Glasgow G12 8LT, Scotland, UK

1. Introduction

Intrinsic parameter fluctuations associated with discreteness of charge and granularity of matter are now major factor limiting scaling and integration [1,2]. The modelling and simulation of such effects is a vibrant area of research. It becomes very important using modelling and simulations to understand the major sources of intrinsic parameter fluctuations and to predict the magnitude of the corresponding variability in the present and next generations nano-CMOS devices. In this paper we present recent advances made by the Glasgow Device Modeling Group in Drift Diffusion (DD), Monte Carlo (MC) and quantum Nonequilibrium Green's Function (NEGF) simulations of intrinsic parameter fluctuations.

2. DD Simulation of Poli-Si gate Induced Variability

In addition to random discrete doping, line edge roughness and oxide thickness variation, the polycrystalinity of the gate has been also identified as a major source of MOSFET variability [3,4]. However, experimental and simulation studies of this effect have been scarce. The simulations here were carried out with the Glasgow 'atomistic' drift-diffusion device simulator, which has been enhanced to include the pinning of the Fermi level, and enhanced doping, in the polysilicon gate along grain boundaries. In order to introduce a realistic random grain structure in the simulations, a large AFM image of polycrystalline silicon grains have been used. After tracing the grain boundaries random sections of the image corresponding to the device dimensions are used to generate the grain pattern in the gate as illustrated schematically in Fig. 1.

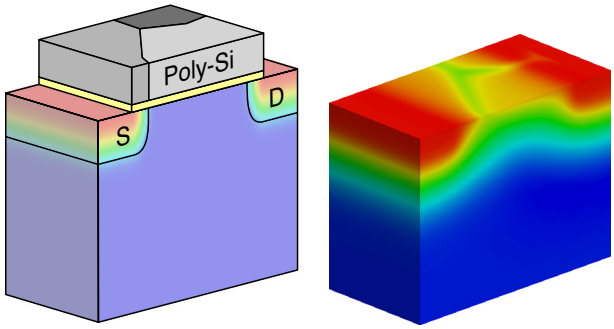

Fig. 1 Schematic of the MOSFET structure simulated, showing different polysilicon grains an the corresponding potential distribution under the gate in the presence of surface potential pinning at the gate grain boundaries.

The band diagram normal to the grain boundary corresponding to a midgap Fermi level pinning is illustrated in Fig. 2. The doping concentration near the grain boundary is also larger due to enhanced diffusion.

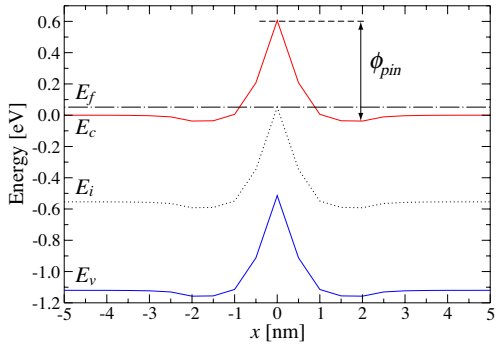

Fig. 2 Midgap Fermi level pinning at a polysilicon grain boundary in the presence of enhanced digffusion.

The simulated dependence of σV_T and $\langle V_T \rangle$ on the average diameter of polysilicon grains is illustrated in Fig. 3 showing a peak in the magnitude of the fluctuations at 30nm average grain size, which corresponds to the dimensions of the MOSFET channel.

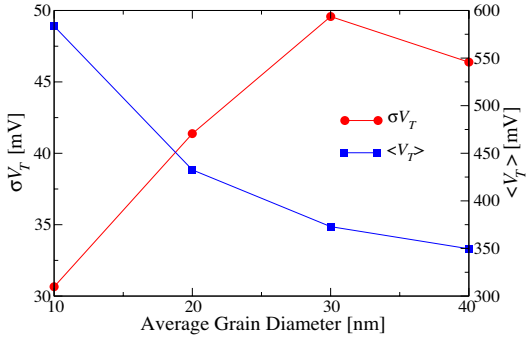

Fig. 3. Dependence of the average threshold voltage, $\langle V_T \rangle$, and the standard deviation of the threshold voltage, σV_T, on the average diameter of the polysilicon grains in a 30×30 nm MOSFET assuming midgap Fermi leviel pining.

3. 'Ab-initio' MC Simulation of On-Current Variability

Random dopants in DD simulations induce variation only through the electrostatic modulation of potential and carrier density associated with the random dopant configuration. However, the same random dopant configuration is also expected to introduce variations through position dependent ionised impurity (II) scattering, which cannot be properly described in the DD framework. In our ensemble 3D MC simulator the II scattering rates are removed from the scattering tables and the II scattering is incorporated directly in *ab-initio* fashion through the real space trajectories of the carriers within the potential associated with discrete dopants. The interaction is estimated using advanced P^3M technique [5]. Fig 4 shows typical electron

concentration and current density distributions obtained from MC at the interface of an atomistic 35 nm MOSFET. Current density is highest in regions with little impurities.

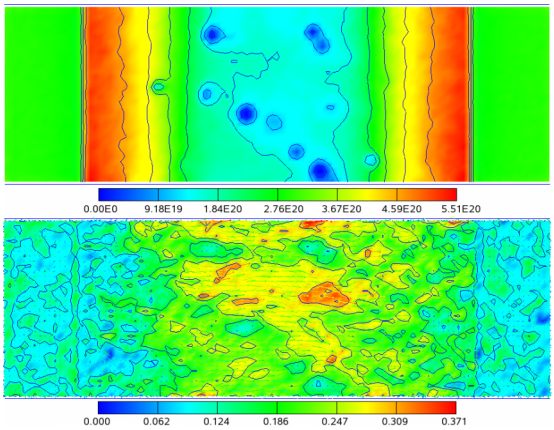

Fig. 4 Electron concentration and current density distribution at the interface of a 35*nm* MOSFET obtained from 3D ensemble MC simulations featuring '*ab initio*' impurity scattering.

The correlation between the on current percentage variation in the above MOSFET obtained from DD and MC simulation is illustrated in Fig. 5. The results of the two types of simulations are well correlated but the MC simulations provide a 4 times large spread in the on current.

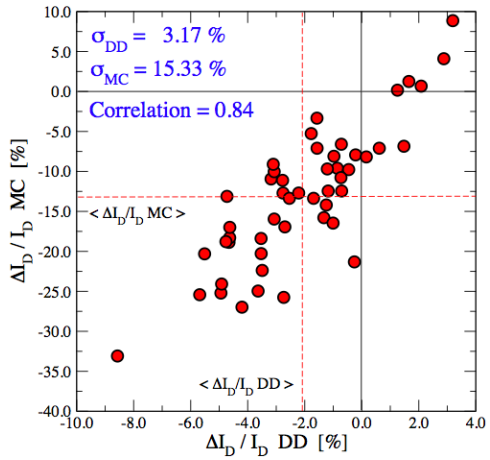

Fig. 5 Variation in current from MC vs. DD simulations of a 35 nm MOSFET. Dashed lines mark the averages of the distributions.

4. 3D NEGF Simulations of interface roughness in nanowire MOSFETS

There are concerns that atomic scale inhomogeneities, such as surface roughness, stray dopants and trapped charges will introduce intolerable variability in nanowire MOSFETs. Previous, studies of such effects have been conducted using 1D Non-Equilibrium Green function (NEDF) transport simulations coupled to transversal states using 'mod-space' approach [6]. In very small nanowire transistors such assumptions are doubtful since surface roughness and discrete defects introduce non-perturbative effects, which greatly distort the transversal wave function leading to a meandering current flow.

Our 3D NEGF simulator employs a recursive algorithm in order to compute efficiently the 3D current and electron density. Control volume discretisation is used to precisely describe the roughness of the surface. We have simulated a gate-all-around nanowire MOSFET with 2×2nm cross-section, 6 nm channel length and 1 nm gate oxide thickness. Fig. 6 shows the potential and current profile in the zy plane for a particular randomly generated interface configuration. In this case the roughness in the surface produces meandering in the current flow.

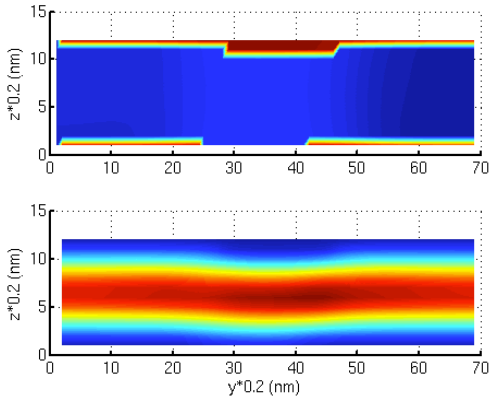

Fig. 6. Nanowire with a random surface roughness producing steps, The potential and current density distributions in the plane x=6nm.

Fig 7 illustrates the I_D-V_G characteristics for a smooth, constricted and meandering nanowires. The constrain results in an extra quantum confinement induced threshold voltage shift.

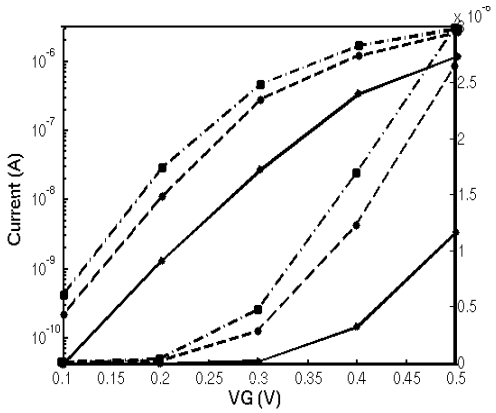

Fig. 7 I_D-V_G characteristics for a smooth, constricted and meandering nanowires.

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