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3D Statistical Simulation of Gate Leakage Fluctuations Due to Combined Interface Roughness and Random Dopants

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1 Introduction

The aggressive reduction of the oxide thickness with scaling results in a dramatic increase in the direct tunnelling gate current (DTGC). The exponential sensitivity of the tunnelling current leads to significant local tunnelling current density variation and gate leakage fluctuations in nano-CMOS transistors. Recent simulation studies identified random discrete dopants (RD) [1] and oxide thickness variation (OTV) [2] as sources of gate leakage fluctuations. However, quantum-confinement effects and bias dependency were not considered and additional research is needed to properly address the problem.

2 Simulation Approach

We have developed a 3D simulation methodology that allows statistical study of the DTGC in realistic nano-MOSFETs. The 3D Glasgow "atomistic" Drift-Diffusion (DD) device simulator with Density Gradient (DG) quantum corrections is at the core of this study [3]. SiO_2/Si interface roughness is constructed using a Gaussian autocorrelation function with 1.8 nm correlation length and 0.28 nm (one interatomic level) RMS height. Random discrete dopants are introduced using a rejection technique based on the concentration ratio between the dopants and the silicon, and scanning site by site the silicon lattice in the transistor [4]. Direct tunnelling current density is modelled based on an improved WKB approximation [5]. The approach is modified to take into account the DG formalism. 1D simulations, based on a self-consistent solution of the Poisson and DG equations, are used to calibrate the modified model to relevant experimental data for inversion and accumulation, as shown in Fig 1 and Fig 2. A non-parabolic, Franz-type band-gap dispersion relation is used for the SiO_2 with a band-edge effective mass $0.72m_e$ (the only fitting parameter).

3 Results and discussion

The described approach was applied to simulate the gate leakage fluctuations in an ensemble of 200 microscopically different MOSFETs with 25 nm gate length and width, 1.0 nm SiO_2 thickness, 5 nm S/D extension overlap, 5×10^{18} cm^{-3} $p-$Si(100) substrate doping level, 1×10^{20} cm^{-3} $n+$poly gate and $n-$Si S/D contacts doping level.

Discrete random dopants and SiO_2/Si interface roughness were simultaneously introduced to study their combined effect on the DTGC.

A sub-sample of the simulated $I_G - V_G$ and $I_G - V_D$ characteristics are illustrated in Fig 4 and Fig 5 respectively. The increase in the mean value of the DTGC in both cases reflects the exponential dependence of the tunnelling current on the oxide thickness. Histograms of the gate leakage current variations in ON-state and OFF-state conditions, relevant for digital circuits operation, are illustrated in Fig. 3 and Fig. 6, and the spread of values is found to be well characterised by a Gaussian distribution. The DTGC fluctuations at high gate voltage are primarily due to the Si/SiO_2 interface roughness, as the effect of the discrete dopants is screened by the excess of electrons in the channel and in the contact extention overlaps. A direct correlation between the tunnelling current density and the features of the oxide interface is illustrated in Fig 7. The DTGC fluctuations at high drain voltage are almost two orders of magnitude and are mainly due to the unique number and configuration of impurity atoms in the drain extension overlap region. Fig.5 illustrates the correlation between the gate current density and the position of the discrete dopants close to the oxide interface.

4 Conclusions

3D statistical simulations of the combined effects of random discrete dopants and oxide thickness variation on the direct tunnelling gate current in a nano-MOSFET were performed. OTV is the primary source of gate leakage fluctuations at high gate voltage (MOSFET "ON" state), while RD are the main factor at high drain voltage (MOSFET "OFF" state). OTV and RD also lead to an average increase in the magnitude of the gate leakage with respect to that of a uniform device. This reflects the exponential sensitivity of the direct tunnelling current, and must be taken into account for accurate power dissipation analysis. A normal distribution represents well the spread of gate current magnitudes, or the spread of Log_{10} of the magnitudes, for the simulated ensemble in both "ON" and "OFF" state of operation. Gate leakage fluctuations in the latter case reach nearly two orders of magnitude. The phenomena studied here are also relevant to devices with oxinitride dielectric.

References

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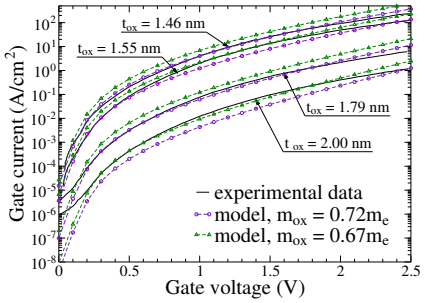

Fig. 1: 1D simulation results and measured data, [6], of DTGC density for a set of large-area MOSFETs in inversion. For all devices, the doping levels of the n+poly gate and the p−Si (100) substrate are $1 \times 10^{20} cm^{-3}$, and $5 \times 10^{17} cm^{-3}$ respectively; the oxide thicknesses are indicated.

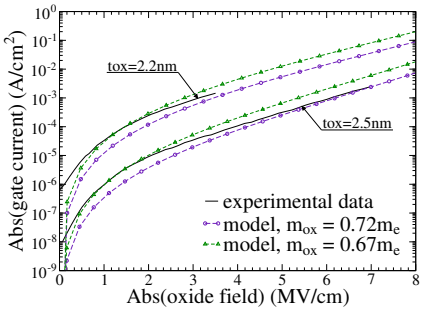

Fig. 2: 1D simulation results and measured data, [5], of DTGC density for a set of large-area MOSFETs in accumulation. For all devices, the p−Si(100) substrate doping level is $5 \times 10^{17} cm^{-3}$; the oxide thicknesses are indicated. The n+poly gate is modelled as n−Si(110) with a doping level $1 \times 10^{20} cm^{-3}$.

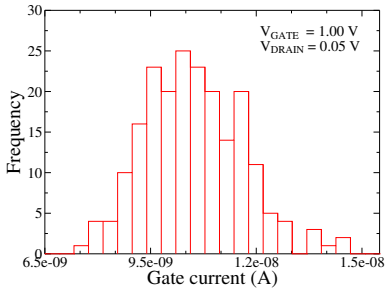

Fig. 3: Gate current histogram for an ensemble of 200 devices with simultaneous OTV and RD. A Gaussian distribution with mean value $\langle I_G \rangle = 1.1 \times 10^{-8}$ and standard deviation $\sigma = 1.4 \times 10^{-9}$ was fitted. The bias condition corresponds to the MOSFET ON-state.

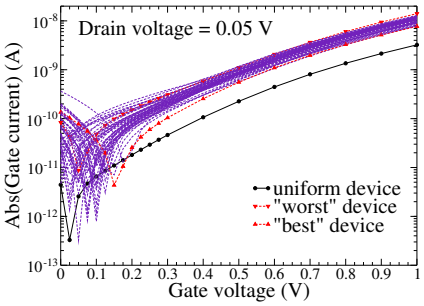

Fig. 4: Simulated $I_G - V_G$ characteristics for an ensemble of 50 devices with simultaneous OTV and RD. The $I_G - V_G$ curve for the uniform device (continuous doping profile and flat interfaces) is shown too.

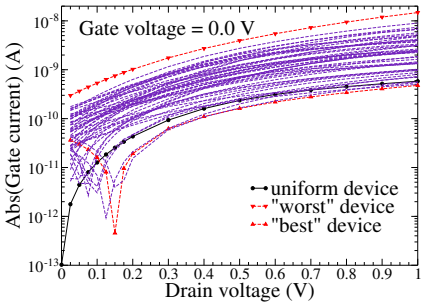

Fig. 5: Simulated $I_G - V_D$ characteristics for an ensemble of 50 devices with simultaneous OTV and RD. The $I_G - V_D$ curve for the uniform device (continuous doping profile and flat interfaces) is shown too.

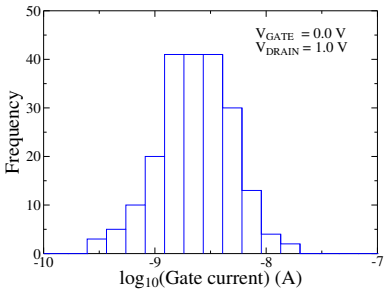

Fig. 6: Gate current histogram for the same ensemble of devices with simultaneous OTV and RD. A Gaussian distribution with mean value $\langle log_{10}(I_G) \rangle = -8.6$ and standard deviation $\sigma = 0.3$ was fitted. The bias condition corresponds to the MOSFET OFF-state.

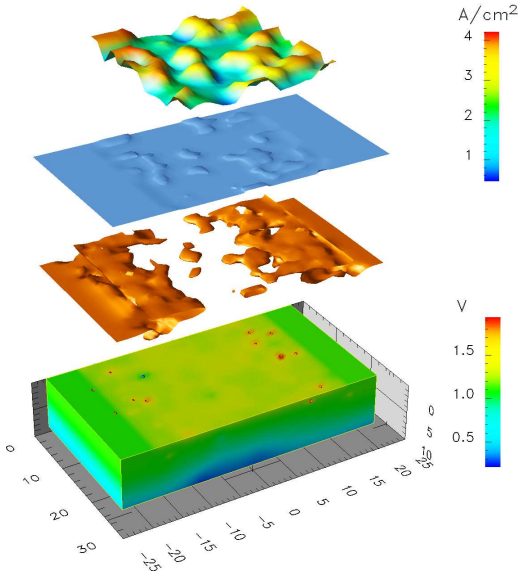

Fig. 7: Typical DTGC density (top, log_{10} of the magnitude), SiO_2/Si surface profile, electron concentration iso-surface (5×10^{19} cm^{-3}, and electrostatic potential (bottom) in the 25 nm gate length MOSFET. $V_G = 1.0$ V and $V_D = 0.05$ V.

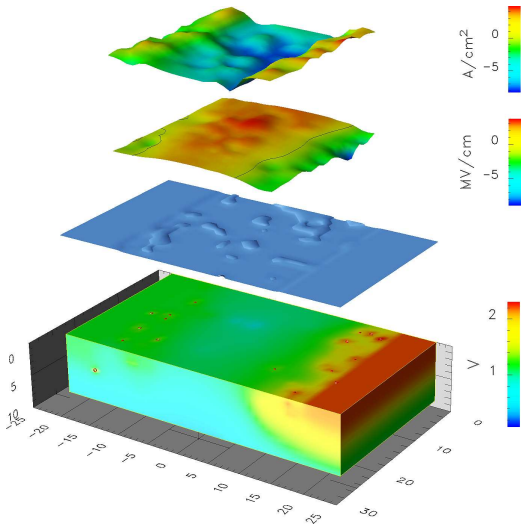

Fig. 8: Typical DTGC density (top, log_{10} of the magnitude), magnitude of the oxide field perpendicular to the SiO_2/Si interface, SiO_2/Si interface surface profile, and electrostatic potential (bottom) in the 25 nm gate length MOSFET studied here. $V_G = 0.0$ V and $V_D = 1.0$ V.