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NBTI Improvement under Highly Compressive Contact Etching Stop Layer (CESL) for 45nm Node CMOS and Beyond

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Abstract

Instead of the complex and high cost SiGe refill scheme, up to 50% drive current enhancement of pMOSFETs has been successfully demonstrated by a highly compressive SiN contact etch stop layer (CESL). Unfortunately, NBTI and TDDB would be degraded due to higher hydrogen from the CESL. In this study, we first proposed that upon application of a modulated buffer layer prior to a highly compressive CESL deposition, the hydrogen could be effectively screened and NBTI and TDDB were also significantly improved without adverse impact on the current enhancement for pMOSFETs. Moreover, the NBTI lifetime for core pMOSFETs could be remarkably improved by over two orders of magnitude.

Introduction

To extend CMOS physical limit, local strain techniques with tensile and compressive nitride CESL layers have been introduced to improve electron mobility and hole mobility, respectively, in the channel region [1-3]. However, most previous literatures focused on the benefits of mobility enhancement on core devices, while much less work was aimed at investigating device reliability. Unfortunately, worse NBTI and TDDB have also been observed after a highly compressive nitride CESL was applied to achieve mobility enhancement in the pMOSFETs' channel [4-7]. It has been reported [7,8] that the physical mechanism of reliability degradation is due to higher content of Si-H and N-H bonds from the compressive nitride CESL film [7]. How to overcome the barrier becomes a challenge for 45nm node CMOS and beyond.

In this study, 50% drive current gain of pMOSFETs has been achieved by optimizing the SiN compressive CESL. However, we addressed a modulated buffer layer with low thermal budget (<450^{0}C), used as a buffer layer to substantially suppress hydrogen incorporation from the highly compressive nitride CESL film. Results reveal that good NBTI and TDDB for pMOSFETs were obtained and the NBTI lifetime could be improved by over two orders of magnitude without adverse impact on the current enhancement of pMOSFETs.

Device Preparation

A high performance CMOS device was fabricated with a dual-oxynitride gate process of 58Å and 12Å physical thickness. After gate patterning, the transistors were integrated with shallow extensions and S/D implants, followed by a rapid thermal anneal. A highly compressive nitride CESL was introduced to enhance the channel strain for pMOSFETs. Before the highly compressive nitride CESL was deposited, on the other hand, a thin modulated buffer layer with low thermal budget below 450^{0}C was first applied to improve the reliability of NBTI and TDDB for pMOSFETs. With the thin modulated buffer layer, there was no adverse impact on the channel strain. **Figure 1** shows a TEM cross-section of pMOSFETs with a modulated buffer layer.

Results and Discussion

I. Transistor Characteristics

Instead of the high cost and complex SiGe refill scheme, up to 50% drive current enhancement of pMOSFETs has been successfully demonstrated by introducing a highly compressive CESL (**Fig. 2**). The results indicate that the high stress CESL is still appropriate for 45nm node CMOS and beyond. As an enough thin buffer layer-A was first introduced prior to the CESL film deposition, there was no adverse impact on the drive current enhancement for pMOSFETs, shown in **Fig. 3(a)**. The drive current gains with different compressive CESL thickness as a function of buffer layer thickness are described in **Fig. 3(b)**. Less performance enhancement of core pMOSFETs has been observed as the thickness of the buffer layer was increased above a critical thickness-B. For IO pMOSFETs, the electrical characteristics Id-Vd are shown in **Fig. 4** and the current enhancement with a highly compressive CESL was insensitive to the buffer layer thickness. **Fig. 5** illustrates C-V characteristics for IO pMOSFETs with and without a buffer layer. The results from C-V characteristics indicated that the process with a modulated buffer layer would not induce extra charges trapping in the oxide bulk.

II. NBTI and TDDB Characteristics

FTIR spectra show that the Si-H and N-H density of the compressive SiN CESL is higher than those of ILD oxide, as shown in **Fig. 6**. Furthermore, the higher concentration of Si-H and N-H would induce serious degradation of NBTI, as shown in **Fig. 7**. **Figure 8** illustrates the relationship between buffer layer thickness and NBTI characteristics for IO pMOSFETs. After stressing at Vg=-4.4V, 120C for 6000secs, serious ΔVt shift of IO pMOSFETs could be observed without a buffer layer. As a very thin buffer layer-A was applied prior to the deposition of a highly compressive CESL, ΔVt shift could be effectively suppressed. The buffer layer can be considered as a barrier to effectively screen the hydrogen diffusion from the compressive SiN CESL layer. **Figure 9** shows the normalized lifetime as a function of Vg for core pMOSFETs with and without a buffer layer. Over two orders of magnitude of lifetime improvement could be achieved by the presence of the very thin buffer layer-A where there is no adverse impact on device performance enhancement. Moreover, much improvement of NBTI could be observed as the buffer layer thickness increased. The TDDB characteristics of IO pMOSFETs with a buffer layer were also improved, as shown in **Fig. 10**. Similar results have also been obtained by core pMOSFETs (not shown here).

Furthermore, the charge pumping results from IO pMOSFETs are also shown in **Fig. 11**. Based on the results, a lower initial charge pumping current has been observed by the sample without a buffer layer and it indicates a low interface state. After stressing at Vg=-4.4V, 120C for 6000secs, however, the interface state without a buffer layer became seriously degraded. It is believed that weak Si-H bonds at interface state were formed from the compressive SiN CESL and the weak Si-H bonds could be easily broken by a highly electrical field stressing [7]. On the other hand, the modulated buffer layer could provide a barrier to screen hydrogen diffusion and further improve the reliability of pMOSFETs.

Conclusions

Instead of the complex SiGe refill scheme, 50% drive current enhancement of pMOSFETs with a compressive SiN CESL has been successfully applied for 45nm node CMOS and beyond. However, hydrogen incorporation from the compressive nitride CESL film must be substantially suppressed to solve the reliability degradation of NBTI and TDDB. In this study, a thin modulated buffer layer prior to the CESL deposition has been first demonstrated to improve the reliability of NBTI and TDDB without adverse impact on the drive current enhancement. Moreover, the NBTI lifetime for core pMOSFETs could be improved by over two orders of magnitude.

References

[1] K. Mistry, et al., pp. 50, *VLSI*, 2004. [2] R. Khamankar, et al., pp. 162, *VLSI*, 2004. [3] V. Chan, et al., pp. 3.8.1 *IEDM*, 2003. [4] F. Ootsuka et al., pp.575, *IEDM*, 2000. [5] T. Enda et al., pp.117, *VLSI*, 2001. [6] J.R. Shih, et al., pp.612, *IRPS*, 2003. [7] H.S. Rhee, et al., pp.709, *IEDM*, 2005. [8] M. Yamamura, et al., pp.88, *VLSI*, 2005.

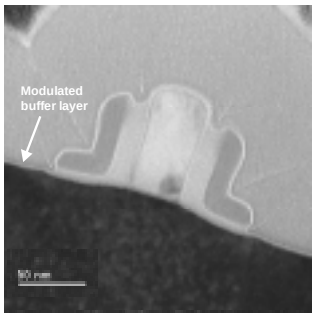

Fig. 1 TEM cross-section of pMOSFET with a thin modulated buffer layer.

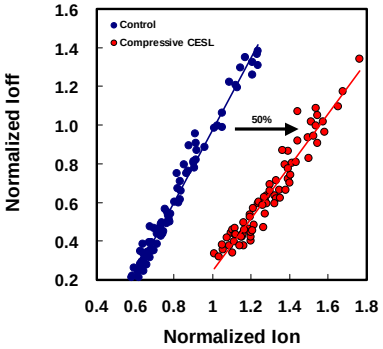

Fig. 2 50% drive current enhancement of pMOSFETs with a highly compressive CESL.

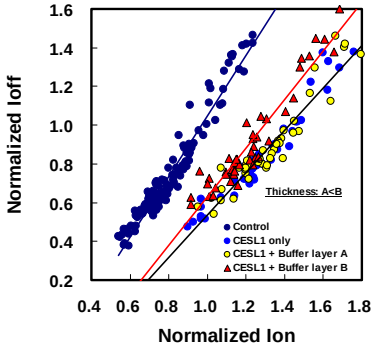

Fig. 3(a) Ion vs. Ioff of pMOSFETs with a high compressive CESL as a function of buffer layer thickness.

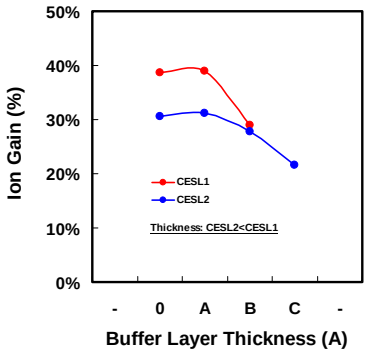

Fig. 3(b) Ion gain dependence of various buffer laver thickness (thickness: A < B <C).

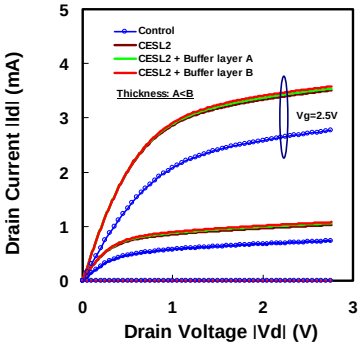

Fig. 4 Typical Id-Vd characteristics of IO pMOSFETs with and without a thin modulated buffer layer.

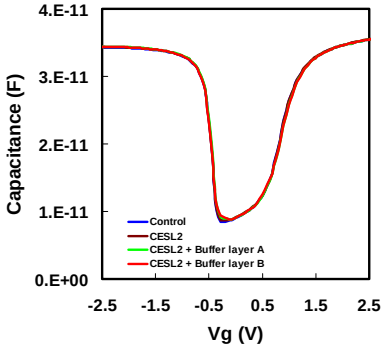

Fig. 5 C-V characteristics of IO pMOSFETs with various buffer layer thickness.

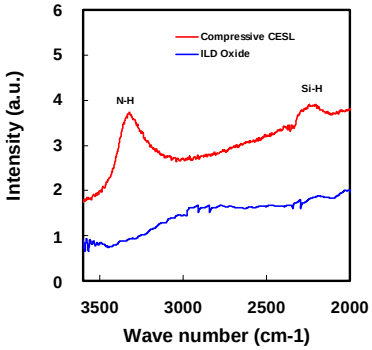

Fig. 6 FTIR spectra of compressive SiN CESL and ILD oxide.

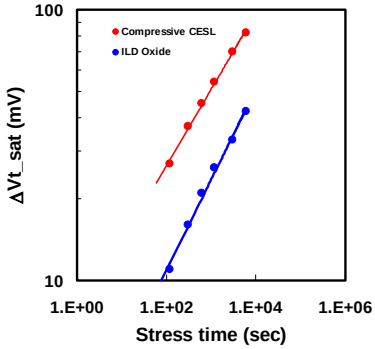

Fig. 7 ΔVt of IO pMOSFETs with and without compressive SiN CESL, stressing at Vg=-4.4V, 125^{0}C.

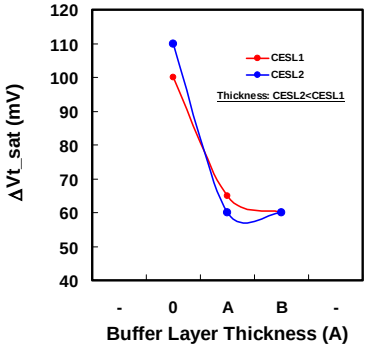

Fig. 8 ΔVt of IO pMOSFETs with stressing at Vg=-4.4V, 125^{0}C for 6000", as a function of buffer layer thickness.

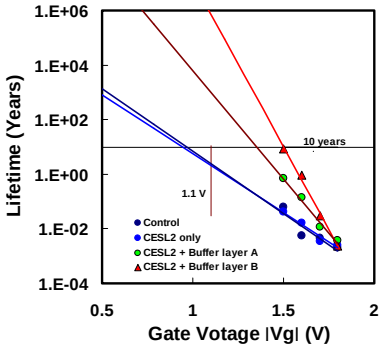

Fig. 9 NBTI lifetime of core pMOSFETs dependence on various modulated buffer layer thickness (thickness: A < B).

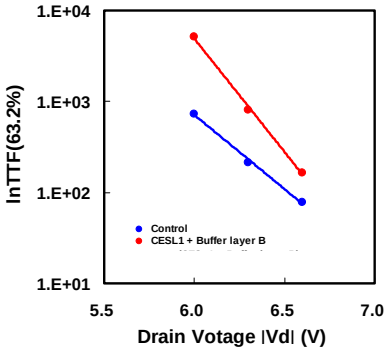

Fig. 10 TDDB comparison of IO pMOSFETs with and without a modulated buffer layer.

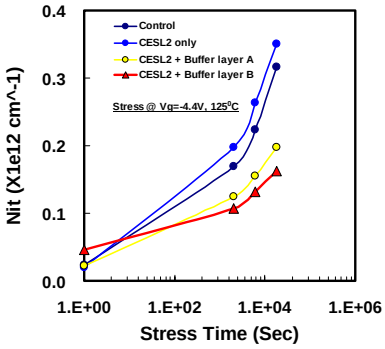

Fig. 11 Nit as a function of stress time from measured I_{CP} curves. The Nits with a buffer layer are less sensitive to the stress.