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NBT Stress Induced Anomalous Drain Current Instability in HfSiON pMOSFETs Arising from Bipolar Charge Trapping

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Abstract

Anomalous negative bias temperature instability (NBTI) in pMOSFETs with HfSiON gate dielectric is presented. Drain current enhancement is obtained in certain NBT stress conditions, giving rise to a turn-around characteristic of drain current change versus stress time and stress V_g. A physical model incorporating bipolar charge trapping in HfSiON during NBT stress is proposed. Post-stress electron emission and hole emission from trap states in high-k gate dielectric are observed due to the bipolar charge trapping.

Introduction

The NBTI in high-k (HK) gate dielectric pMOSFETs is less studied [1,2], compared to their n-type counterparts. We have shown that HK charge trapping/detrapping in a switching delay (up to seconds) between stress and sense in a conventional measurement method is significant [3-5] To retrieve the lost information between stress and I_d sensing, a fast transient measurement technique [4] is utilized in this work. An anomalous NBT stress induced I_d *enhancement* is observed. A physical model based on bipolar charge trapping in HK gate dielectric is proposed to explain the observed phenomena.

The HfSiON pMOSFETs used in this work have a gate length of 0.08~1.2μm and a gate width of 0.16~10μm. NBT stress at V_g/temperature=-1.2V~-2.8V/25C~125C is applied. The linear drain current ($I_{d,lin}$) is measured at V_g/V_d=-1.2V/-0.2V to evaluate the NBTI effect.

Results and Discussion

(a) I_d Enhancement and Degradation:

Fig. 1 shows the stress time dependence of $\Delta I_{d.lin}$ at different stress V_g and temperatures. A turn-around characteristic of $\Delta I_{d.lin}$ is observed at a larger $|V_g|$ and/or higher temperature stress. Fig. 2 and Fig. 3 show the $\Delta I_{d.lin}$ versus stress V_g and temperature. For a shorter stress time (t<10s), an anomalous I_d enhancement is obtained in certain stress conditions. But for a longer stress time (e.g., t=1000s), $\Delta I_{d.lin}$ is always negative and the drain current degradation increases monotonically with stress V_g and temperature. It should be mentioned that a conventional measurement method, which has a switching delay on the order of seconds, may fail to observe the abnormal I_d enhancement.

(b)Bipolar Charge Trapping Model: Two carrier injection processes in NBT stress affect I_d instability: (i) trapping of valence electrons injected from p^+ poly-gate into HK traps ($\Delta I_{d.lin}$>0) and (ii) trapping of holes from the inverted channel into HK or interfacial SiO_2 layers (IL) ($\Delta I_{d.lin}$<0). Fig. 4 illustrates the band diagrams before stress (Fig. 4(a)) and in different stress conditions (Fig. 4(b-d)). In Fig. 4(a), the device is in thermal equilibrium and HK trap states below the Fermi level (E_F) are occupied by electrons. The shaded area in Fig. 4 represents the occupied trap states. At a low stress $|V_g|$/temperature (Fig. 4b), the empty HK traps available for poly-gate valence electron tunneling are very limited due to a small band-bending. In this case, electron trapping is negligible and $\Delta I_{d.lin}$ is dominated by hole injection from the channel. As stress temperature or stress $|V_g|$ increases, more poly-gate electrons can inject into pre-existing HK dielectric traps either by thermally assisted tunneling (Fig. 4(c)) or because of more available empty traps due to a larger band-bending (Fig. 4(d)). In these conditions, both electron trapping and hole trapping in HK gate dielectric are possible. Electron trapping is dominant in the initial stress period and hole trapping gradually supersedes electron trapping due to new hole trap creation in HK and IL layers, giving rise to a turn-around feature of $\Delta I_{d.lin}$ in Figs.1-2.

(c) Measurement of Single Charge Emission: Direct measurement of single trapped charge emission from dielectric traps in a recovery period has been reported in our previous papers [3,4]. Fig. 5 shows typical recovery I_d patterns after low (-1.5V) and high (-2.2V) $|V_g|$ stress. The purpose of this measurement is to identify injected charge species during stress. An upward current jump in Fig. 5 corresponds to a single hole detrapping and a downward jump corresponds to a single electron detrapping. Only trapped hole emission is found for the low $|V_g|$ stress (Fig. 5(a)), while both electron and hole emissions are observed for the high $|V_g|$ stress (Fig. 5(b)). *This measurement result provides direct evidence for bipolar charge trapping in high $|V_g|$ stress.* In addition, we measure a charge pumping (CP) current in low and high $|V_g|$ stress (Fig. 6). A two-frequency technique is used to separate IL/Si interface traps (D_{it}) and bulk HK traps (N_{HK}) [6]. Our CP result shows no new traps are created in low V_g (-1.5V) stress even for t=1000s, indicating that the I_d degradation is mainly attributed to hole trapping in pre-existing HK traps. On the other side, both interface trap and bulk HK trap generation is observed in high V_g (-2.2V) stress.

Conclusions

The impact of stress V_g, temperature, and stress time on NBTI in HfSiON pMOSFETs is investigated. Bipolar charge trapping in HK dielectric by NBT stress is observed by using our fast transient measurement method. The drain current instability modes are summarized in Table I. At high $|V_g|$ and/or high temperature stress, electron trapping into pre-existing HK trap is dominant in the initial stage, thus causing an I_d enhancement. As stress continues, hole injection and new hole trap creation in HK/IL layers eventually becomes dominant. For low $|V_g|$ stress, the I_d instability is dictated by hole injection only throughout the entire stress period.

References
[1] S. Zafar, et al., VLSI Tech. 2004, pp.208-209
[2] M. Houssa, et al., VLSI Tech. 2004, pp.212-213
[3] C. T. Chan, et al., IRPS 2005, pp.41-44
[4] C. T. Chan, et al., VLSI Tech. 2005, pp.90-91
[5] C. T. Chan, et al., IEDM 2005, pp.563-566
[6] R. Degraeve, et al., IEDM 2003, pp.935-938

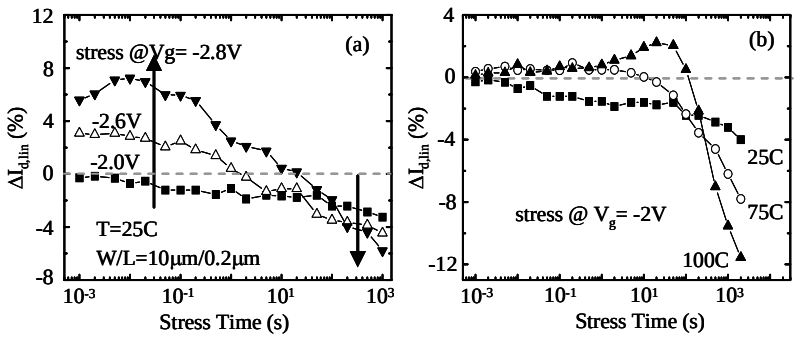

Fig. 1 NBT stress induced drain current change. (a) stress V_g effect, and (b) stress temperature effect. Anomalous current enhancement during initial stage of stressing is observed for high T and high $|V_g|$.

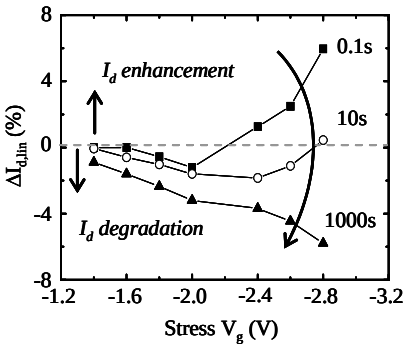

Fig. 2 Stress V_g dependence. For a short stress time (t=0.1s and 10s), the $\Delta I_{d,lin}$ can be positive or negative, depending on stress V_g. For a prolonged stress time (t=1000s), a negative $\Delta I_{d,lin}$ is obtained (I_d degradation).

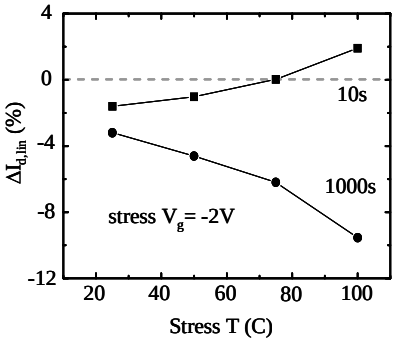

Fig. 3 Stress temperature dependence. For a short stress time (t=10s), $\Delta I_{d,lin}$ changes from a degradation at low stress temperature to an enhancement at high stress temperature.

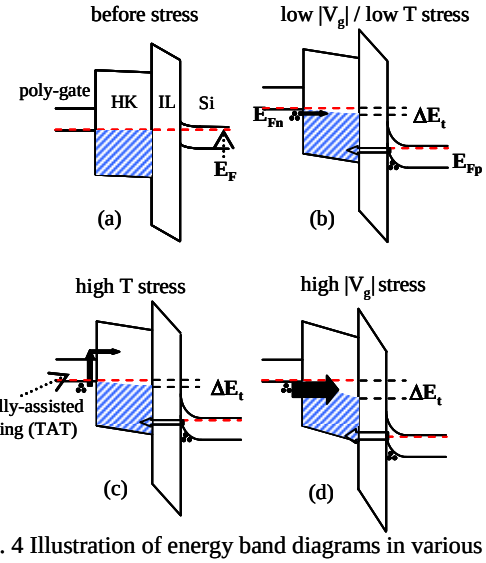

Fig. 4 Illustration of energy band diagrams in various conditions (a) thermal equilibrium (before stress), (b) low $|V_g|$/low temperature stress, (c) low $|V_g|$/high temperature stress, and (d) high $|V_g|$/low temperature stress. The shaded area represents occupied trap states. Thermally assisted tunneling is shown in Fig. 4(c).

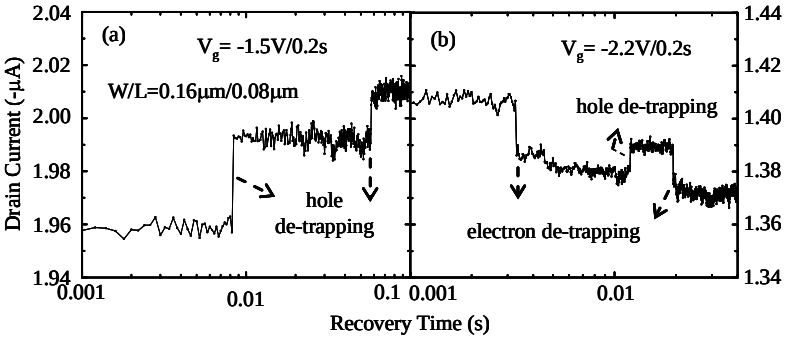

Fig. 5 The recovery drain current transient immediately after NBT stress. The NBT stress time is 0.2s. (a) Stress V_g= -1.5V and (b) stress V_g= -2.2V. The discontinuous current change corresponds to a single trapped charge emission.

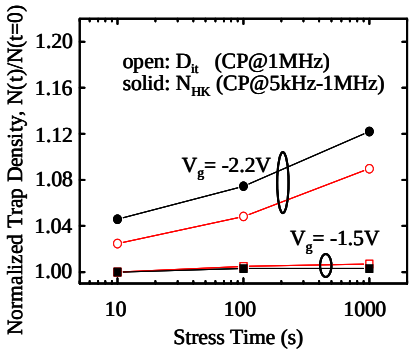

Fig. 6 Interface traps (D_{it}) and bulk HK traps (N_{HK}) growth rates for NBT stress at V_g= -1.5V and -2.2V and T=25C. A two-frequency charge pumping measurement technique is used.[6]

Table 1. Summary of NBT stress caused drain current instability and responsible mechanisms.

Stress Time \ Stress $\|V_g\|$ and T	low $\|V_g\|$	high $\|V_g\|$	high temperature
short	1.Hole trapping into HK traps 2.I_D degradation	1.Electron trapping into HK traps 2.Hole trapping into HK traps 3.I_D enhancement	1.Electron trapping into HK traps via thermally assisted tunneling 2.Hole trapping into HK 3.I_D enhancement
long	1.Hole trapping 2.HK/IL degradation 3.I_D degradation	1.Electron/ hole trapping 2.HK/IL degradation 3.I_D degradation	1.Electron/ hole trapping 2.Accelerated HK/IL degradation 3.I_D degradation