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Impact of Silicon Film Thickness on LF Noise in SOI Devices

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Abstract

In this paper the impact of the film thickness is studied for different SOI devices.

1. Introduction

SOI devices seem to be an attractive solution for miniaturizing and integrating systems. As the device length reduces, the silicon film thickness (t_{si}) of these devices decreases as well. The effect of this reduction needs to be carefully characterized. The low frequency (LF) noise, being a serious concern for RF and analog designs, is as well a powerful diagnostic tool, giving an insight over the carrier behaviour concerning the Si/dielectric interface. In this paper the LF noise of SOI devices with different film thickness is studied and compared varying the front and back gate voltages.

2. Results and Discussions

Partially Depleted (PD), Fully Depleted (FD) and Double Gate (DG) SOI CMOS technologies are studied. The front gate oxide is 2nm for all devices. In the PD SOI, t_{si} is 60nm and the back gate oxide thickness (t_{BOX}) is 400nm. Two types of FD SOI are used: FD devices with HfO_2/Tin gate stack, 10nm silicon film thickness and 145nm t_{BOX}, and FD devices with SiO_2 as the dielectric, 15nm tsi and 400nm t_{BOX}. The DG devices have 6nm film thickness. Noise measurements were carried out in the 1Hz to 100 kHz frequency range using a fully automatic LF noise measurement system. Different front and back gate voltages have been applied.

Regarding Figs.1, 3, 4, 5, we observe a correlation between the normalised drain current power spectral density, S_{Id}/I_d^2 and $(gm/I_d)^2 \times S_{VG}$ for all devices which confirms the results predicted by the 1/f noise model on carrier number fluctuations [1].

Partially Depleted SOI with t_{si}=60nm

In Fig.2 the drain current power spectral density for Vg_1 =0.8V shows a Lorentzian spectrum for the accumulation mode of the back gate. It should be noted that the applied Vg_1 is below the EVB tunnelling threshold [2] which explains the 1/f spectrum for Vg_2=0V. The excess Lorentzian noise can be explained by the fact that, while increasing the negative back gate bias, the source/body and body/drain current increases by tunnelling through the back-gate-induced p+ n+ junctions thereby increasing the shot and thermal noise [4]. Taking into account the model explaining the shot noise induced excess LF noise in PD devices [3], this means giving rise to a Lorentzian-like spectral density in noise.

Fully Depleted SOI with t_{si}=15nm

The impact of Vg_2 in Fig.3 can be explained by the fact that when the back gate is accumulated, the carrier number fluctuations induced by the back oxide traps are screened by the accumulation layer, the FD device behaves as a bulk CMOS, whereas when depleting the back interface, the noise becomes higher due to the coupling effect [5].

Fully Depleted SOI with t_{si}=10nm

As can be seen in Fig.4 depleting the back interface, does not change the noise level when the front interface is in weak inversion. The rather thin film in these devices suggests that the inversion charges could be pushed away from both interfaces by depleting the back interface, which could compensate the increase due to the coupling effect in the noise level. When the front interface is in strong inversion, the noise level for back interface in depletion mode reduces which is due to the reduction of the Coulombic scattering parameter [6]. The increase of the noise level for back interface in accumulation mode is partly due to the HfO_2/TiN gate stack.

Double Gate SOI with t_{si}=6nm

Since the silicon film is very thin, when depleting the back interface, the charge is pushed away from both interfaces and the number of trapped carriers is reduced due to the screening thereby reducing the noise level (Fig.5). The exponent δ of the $1/f^{\delta}$ spectrum in Fig.6 shows a decrease when depleting the back interface which is a proof of a smaller trap profile [7], implying that the carriers are not as close to the interface as they are when Vg_2=0V.

3. Conclusions

The impact of the back gate voltage on the amplitude of the noise depends on the silicon film thickness. For PD devices, back interface accumulation mode has a higher noise level due to a Lorentzian component. Decreasing the thickness, depletion mode of the back interface shows an increase in the LF noise due to the coupling effect. For a FD device with tsi=10nm, depletion mode of the back interface does not have an influence on the noise level due to the compensation of the screening and coupling effect. For tsi=6nm the noise decreases when the back interface is in depletion mode due to the screening effect.

References

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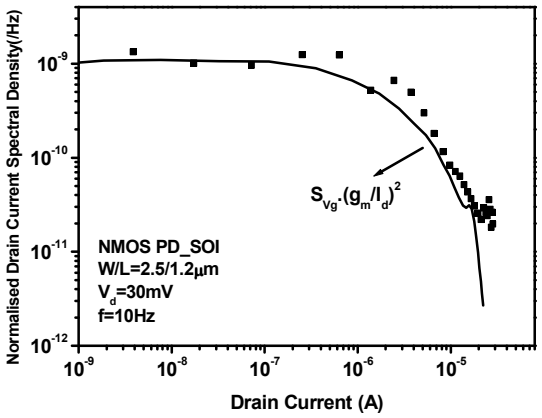

Fig. 1 Normalised drain current spectral density for a PD SOI with W/L=2.5/1.2μm, at Vd=30mV and f=10Hz.

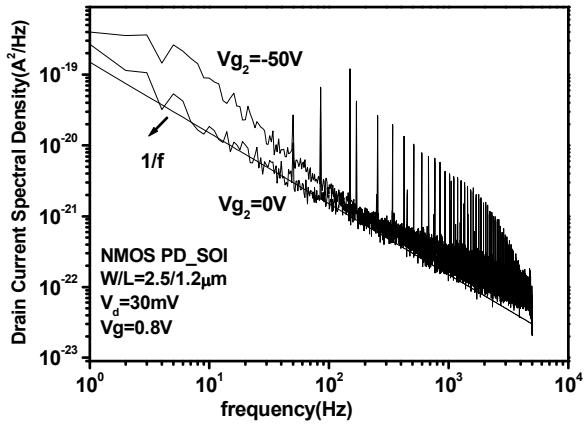

Fig. 2 Drain current spectral density for a PD SOI with W/L=2.5/1.2μm, at Vd=30mV and Vg_1=0.8V for Vg_2=0 and –50V.

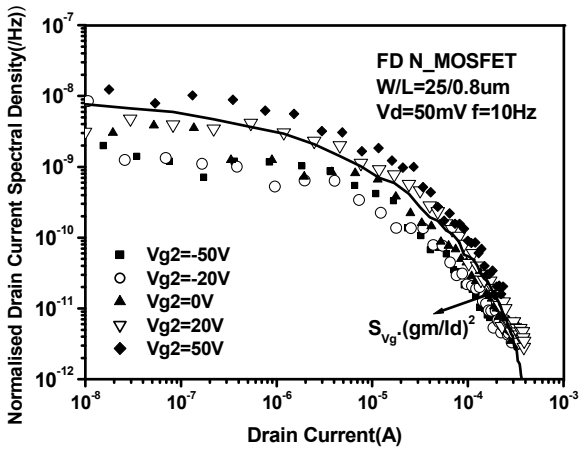

Fig. 3 Normalised drain current spectral density for a FD SOI with W/L=25/0.8μm, at Vd=50mV, f=10Hz and Vg_2=-50…50V.

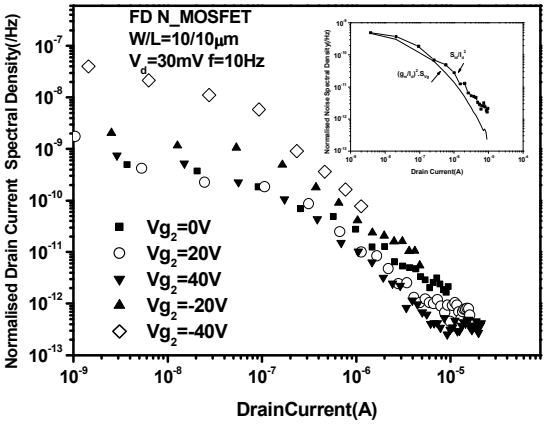

Fig. 4 Normalised drain current spectral density for a FD SOI with W/L=10/10μm, at Vd=30mV, f=10Hz and Vg_2=-40…40V.

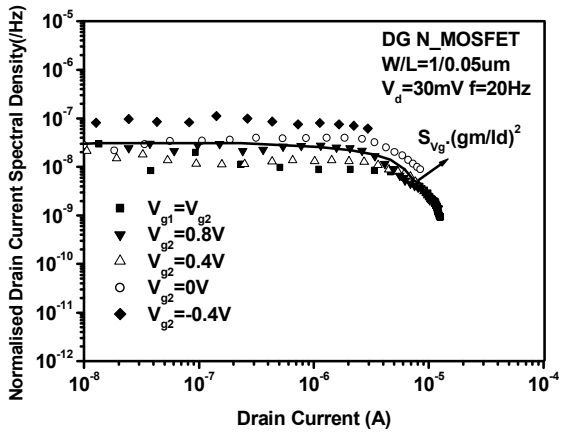

Fig. 5 Normalised drain current spectral density for a DG SOI with W/L=1/0.05μm, at Vd=30mV, f=10Hz and Vg_2=-0.4…0.8V.

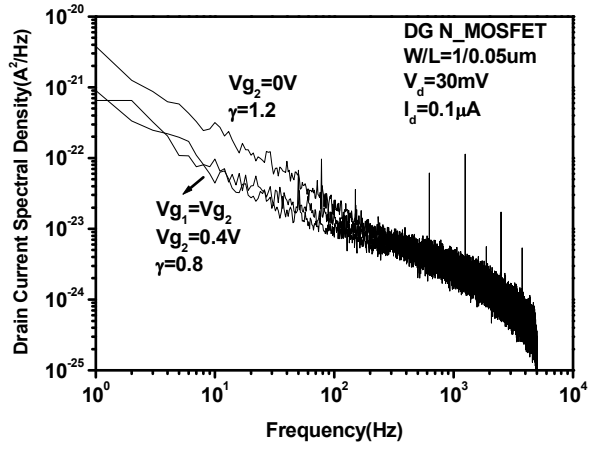

Fig. 6 Drain current spectral density for a DG SOI with W/L=1/0.05μm, at Vd=30mV and Id=0.1μA for Vg_2=0 and 0.4V and also Vg_1 =Vg_2 (double gate mode).