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Comparison of Threshold Voltage Fluctuations in Sub-45 nm Planar MOSFET and Thin-Buried-Oxide SOI Devices

Yiming Li* and Shao-Ming Yu[1]
Department of Communication Engineering, National Chiao Tung University
[1]Department of Computer Science, National Chiao Tung University
1001 Ta-Hsueh Road, Hsinchu City, Hsinchu 300, TAIWAN
*Corresponding Author. Phone: +886-3-5712121 ext. 52974; Email: ymli@mail.nctu.edu.tw

1. Introduction

As the dimension of semiconductor devices shrunk into nanometer scale [1], fluctuations of electrical characteristics are especially pronounced [2-4]. Fluctuation of threshold voltage is crucial for the circuit design; in particular, for the issues of design window, yield, noise margin, stability, and reliability of ultra large-scale integration circuits. Therefore, new planar-compatible transistor structure such as thin-buried-oxide (TBO) SOI [5] has been advanced. Devices fabricated on SOI substrate with thin buried oxide have smaller roll-off of threshold voltage and it can enhance short channel control without scaling gate dielectric thickness.

In this paper, we investigate the fluctuation of threshold voltages for planar MOSFET and thin-buried-oxide SOI devices. To explore fluctuations of threshold voltage in nanoscale devices, we try to classify fluctuation into several components which includes at least three major factors, random doping (RD) fluctuation, gate length (Lg) deviation, and line edge roughness (LER). We analysis these fluctuation factors and compare the results between planar MOSFETs and thin-buried-oxide SOI. We found that thin-buried-oxide SOI has smaller threshold voltage fluctuation, compared with the conventional planar MOSFETs.

2. Methodology

The fluctuation of threshold voltage (Vt) is assumed to be contributed from random dopant, gate length deviation, and line edge roughness. The standard deviation of total threshold voltage, $\sigma_{Vt,total}$, is expressed as

$$\sigma_{Vt,total}^2 = \sigma_{Vt,RD}^2 + \sigma_{Vt,Lg}^2 + \sigma_{Vt,LER}^2,$$

where $\sigma_{Vt,RD}$ is random dopant-induced fluctuation, $\sigma_{Vt,Lg}$ and $\sigma_{Vt,LER}$ are fluctuations caused by gate length deviation and line edge roughness, respectively. Based on our recently work [6-8], we calculate the random doping induced fluctuation $\sigma_{Vt,RD}$ with quantum correction approach by application of perturbation and monotone iterative techniques to quantum transport model at equilibrium conditions for planar MOSFET and TBO SOI [5], shown in Fig. 1. Thus, the variance of the threshold voltage of nanoscale MOSFET and TBO SOI are calculated with respect to different physical quantities including random dopant. This quantum mechanical correction approach successfully considers the effect of the random dopant and structure-dimension effect on the threshold voltage fluctuation. Furthermore, we apply the statistical approaches to evaluate the effect of $\sigma_{Vt,Lg}$ and $\sigma_{Vt,LER}$, and the magnitude of gate length deviation and line edge roughness are extracted from the projections of ITRS roadmap 2005 for different technology nodes. According to a prediction of realistic silicon data, we simulate the Vt roll-off versus Lg, and randomly generate testing sets, where the standard deviation of each set is $3\sigma_{Lg}$ = 1.9 nm for the 45 nm node and $3\sigma_{Lg}$ = 1.3 nm for 32 nm technology node. We then calculate the $\sigma_{Vt,Lg}$ among all testing sets to get the maximum one as our result. With this similar idea, we divide the channel into several sections and randomly assign a length to each section corresponding to CD SEM samples of fabricated devices. The deviation of line edge roughness follows the rule $3\sigma_{LER}$ = 2.4 nm for 45 nm node and $3\sigma_{LER}$ = 1.7 nm for 32 nm node and then $\sigma_{Vt,LER}$ is computed.

3. Results and Discussion

Figure 2 shows the computed Vt fluctuation components for planar poly-gate MOSFET with nominal gate length of 35 nm. In this case, the effects of gate length deviation and line edge roughness exceed random doping fluctuation when Lg less than 25 nm, and dominate the total fluctuations in small gate length. Result shows that the $\sigma_{vt,LER}$ could be about 1.5 times larger than $\sigma_{vt,RD}$. Figure 3 shows the standard deviation of Vt versus the equivalent oxide thickness (EOT) for a 35 nm MOSFET. It is found that when EOT decreases, all the fluctuation components decrease. EOT significantly dominates $\sigma_{vt,RD}$, because EOT decrease implies a better channel controllability. Figures 4 and 5 show a comparison of all fluctuation components for the three different devices. As shown in Fig. 4, metal-gate + high-κ MOSFET can reduce the random dopant-induced fluctuation, so it has a smaller total fluctuation compared with the result of poly-gate MOSFET. Reduction directly attributes to a low channel doping in metal gate structure. From Fig. 5, it is found that effect of Lg on Vt fluctuation is suppressed according to structure's nature. However, $\sigma_{vt,RD}$ is a little bit larger than that of metal-gate + high-κ MOSFET due to existing channel doping. Figure 6 shows a comparison of total fluctuation for poly-gate MOSFET, metal-gate + high-κ (gate material) MOSFET, and TBO SOI devices. The TBO SOI has the smallest fluctuation among all devices due to it has a quasi double-gate structure. Therefore, it not only suppresses the short channel effect but also improves gate channel controllability than that of other two structures.

4. Conclusions

Fluctuation of threshold voltage caused by random dopant, gate length deviation and line edge roughness are explored and compared for nanoscale planar MOSFET and TBO SOI devices. TBO SOI has shown smaller threshold voltage fluctuation for all factors, compared with planar MOSFETs. TBO SOI is promising for sub-32 nm technology. We are currently analyzing and modeling realistic silicon data and exploring fluctuation of static noise margin of SRAM with TBO SOI devices.

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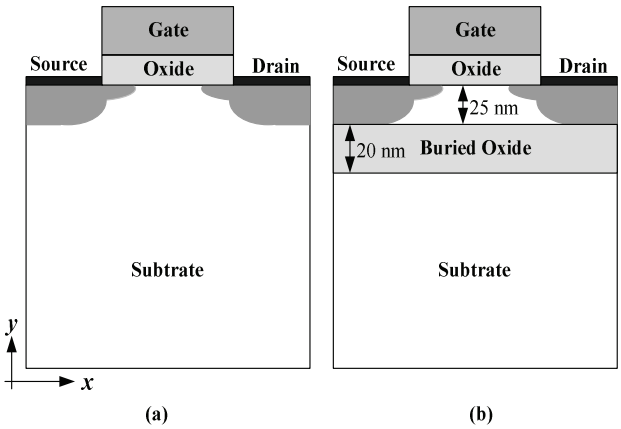

Figure 1. Cross-section views of the studied (a) planar MOSFET and (b) thin-buried-oxide SOI devices. Fluctuation of surface potentials for the explored devise is computed in this study.

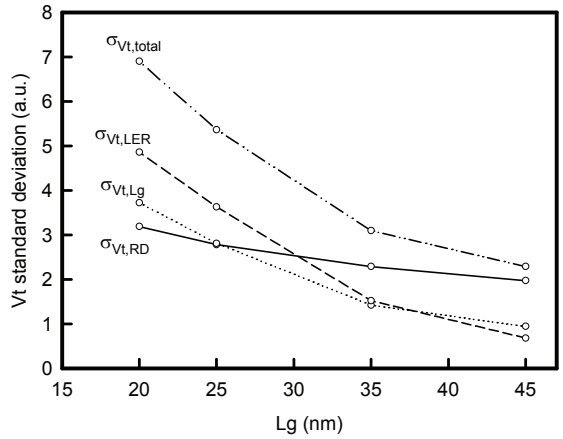

Figure 2. Normalized threshold voltage fluctuation of MOSFET devices. For 45 nm technology node, we assume that the nominal Lg of the device is 35 nm and oxide thickness is 1.7 nm. It includes $\sigma_{vt,RD}$, $\sigma_{vt,Lg}$ and $\sigma_{vt,LER}$, respectively.

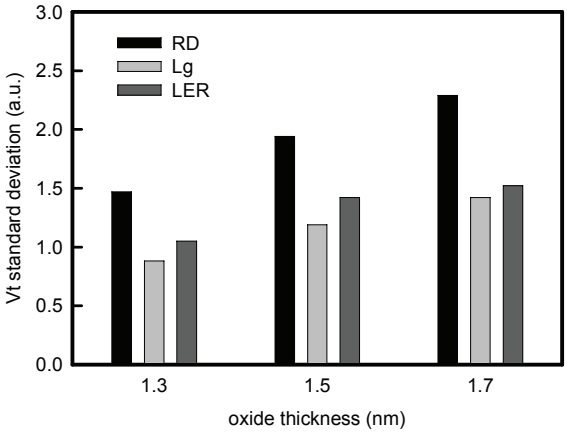

Figure 3. Normalized threshold voltage fluctuation versus the equivalent oxide thickness for a 35 nm MOSFET.

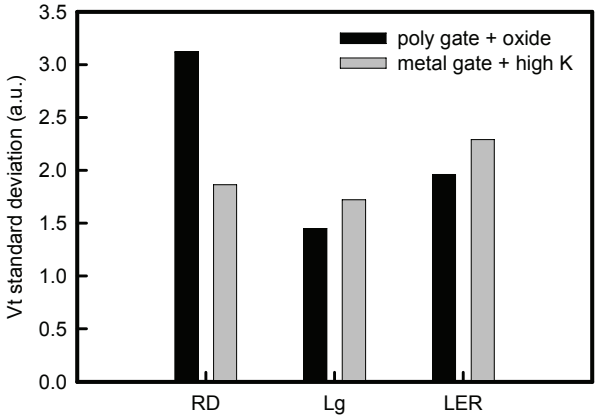

Figure 4. Normalized threshold voltage fluctuation components of poly-gate MOSFET and metal-gate and high-κ materials MOSFET, where Lg is 25 nm and oxide thickness is 1.5 nm for the 32 nm technology node.

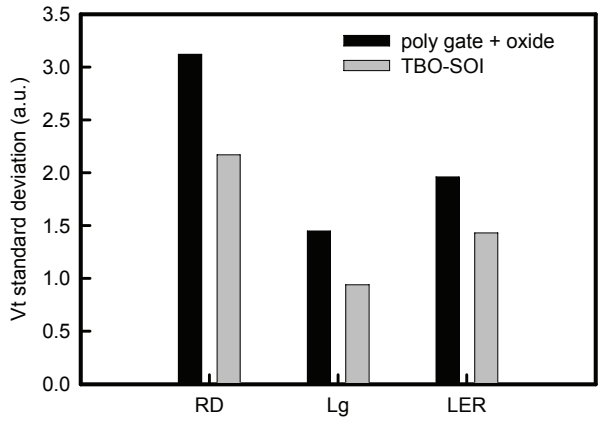

Figure 5. Normalized threshold voltage fluctuation components of poly-gate MOSFET and TBO SOI, where Lg is 25 nm and oxide thickness is 1.5 nm.

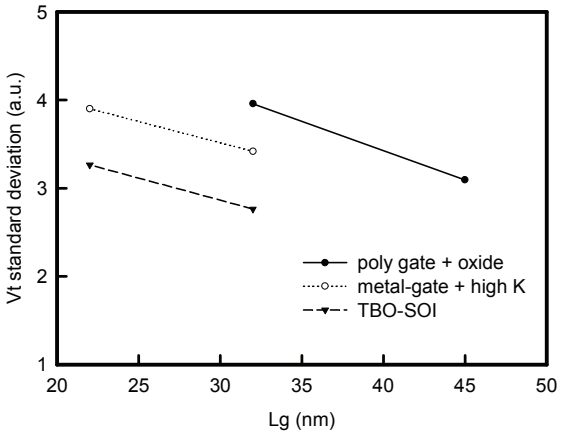

Figure 6. Normalized threshold voltage fluctuation versus the gate length for poly-gate, metal-gate + high-κ MOSFETs, and thin-buried-oxide SOI.