Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 984-985

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High-k HfO_2/Al_2O_3 nanolaminated charge trapping layers for high performance flash memory device applications

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1. Introduction

Due to the poor retention and scaling issue in polysilicon-oxide-silicon-nitride-oxide-silicon (SONOS) flash memory devices [1], the high-κ charge trapping layers such as HfO_2 or HfAlO films in metal-oxide-high-κ-oxide-silicon (MOHOS) structure are demanded for future nano-scaled non-volatile memory (NVM) device applications [2,3]. To improve further the scaling and to increase the program/erase speed, the high-κ material with large barrier height such as Al_2O_3 [3-4] is also interesting alternative as a blocking oxide for high-speed flash memory applications. To obtain a high performance flash memory, the HfO_2/Al_2O_3 nanolaminated charge trapping layers with Al_2O_3 as a blocking oxide in MAHOS (metal-Al_2O_3-high-κ-SiO_2-Si) structure formed by ALD is proposed for the first time. The MAHOS memory devices with different gate electrodes such as Al and Pt are also studied. The pure Al_2O_3 in metal/Al_2O_3/SiO_2 (MAOS) structure is also investigated for comparison.

2. Experimental

The starting wafer was p-type Si (100) with resistivity of 15-25 Ω.cm. Prior to deposition of tunneling oxide (SiO_2), the p-Si wafers were cleaned by diluted HF dip. The high quality tunneling oxide with the thickness of ~3 nm was grown nominally by RTO system at temperature of 1000°C for 20s. Then, pure HfO_2, pure HfAlO (Hf:Al=1:1), nanolaminated HfO_2(1nm)/Al_2O_3(1nm) with 5 periods, and nanolaminated HfO_2(2nm)/Al_2O_3(2nm) with 3 periods of HfO_2 (~2nm) and 2 periods of Al_2O_3 (~2nm) charge trapping layers with total thickness of ~10nm by ALD system using hafnium tetrachloride ($HfCl_4$) and trimethylaluminium ($Al(CH_3)_3$) precursors at substrate temperature of 300°C were deposited on SiO_2 (~3nm-thick) grown p-Si. Then, the Al_2O_3 as a blocking oxide with the thickness of ~10 nm was deposited *in-situ* on the nanolaminated charge trapping layers by ALD. The ~20 nm-thick Al_2O_3 was deposited on SiO_2 (~3nm-thick) treated p-Si substrate for comparison. Now, the nanolaminated HfO_2(1nm)/Al_2O_3(1nm) and HfO_2 (2nm)/Al_2O_3(2nm) charge trapping layers are named as nano1 and nano2, respectively. All as-deposited high-κ films show amorphous and the hysteresis memory windows are not observed. To get the high charge trapping sites as well as memory windows, the post deposition annealing (PDA) treatment at 900°C for 1min in N_2 ambient was performed. After PDA process, the pure HfO_2 film shows fully crystalline and Al_2O_3 or HfAlO shows almost no crystalline or amorphous. The charge trapping layers of nano1 sample shows fully crystalline with different crystal orientations at different positions by TEM analysis after the PDA process (not shown here). After PDA treatment, the nano2 sample shows a double HfO_2 charge trapping layers with HfAlO film as a barrier layer as shown in HRTEM image [Fig. 1(a)]. It is noted that the middle Al_2O_3 (2nm)/HfO_2(2nm)/Al_2O_3(2nm) layers are mixed together resulting the partial crystalline of HfAlO barrier layer. The final structure of nano2 sample is HfO_2(~3.5nm)/HfAlO(~3nm)/HfO_2(~3.5nm) layers after annealing process by HRTEM as well as EDS measurements [Fig. 1(b)]. The HfO_2/HfAlO/HfO_2 charge storage layers are useful to improve the charge retention characteristics of high-density flash memory devices. To study the MAHOS and MAOS device performances, the Al and Pt metals as gate electrodes are used. The post metal annealing with temperature of 400°C and 5 min was done using forming gas ambient.

3. Results and discussion

A large C-V hysteresis memory window (~10V@ V_g=±15V) is observed for nano2 memory devices, due to the charge storage in layer-by-layer (Fig. 2). A schematic band diagram of double HfO_2 charge storage layers under program/erase mode is shown in Fig. 3. To improve the charge retention, the HfAlO layer between the double HfO_2 charge trapping layers is used. The high V_{FB} shift of ~5V (Fig. 4) and high charge trapping density of ~$1.6x10^{13}/cm^3$ (Fig. 5) of nano2 memory device is observed than that of other charge trapping devices. The V_{FB} shift is measured with respect to the V_{FB} of quasi-neutral C-V curve (V_{FBN}). The V_{FBN} is the flat-band voltage from quasi-neutral C-V curve (the sweep gate voltage was V_g~±2V). All MAHOS memory devices show good performance as compared with the MAOS memory devices. It can be explained that the conduction band offset of the HfO_2 film with respect to Si substrate is smaller (~1.7 eV) as compared with the one (~2.8 eV) of the Al_2O_3 film. The value of valence band as well as conduction band offset is confirmed by ultra-violet photoelectron spectroscopy measurement (not shown here). Due to the small conduction band offset (<1.7eV), more electrons can be injected in the HfO_2/Al_2O_3 nanolaminated charge trapping layers from Si substrate because the tunneling current is dominated at the same gate voltage. To erase easily, the high work function metal gate (Pt) is needed (Fig. 6) because the backward tunneling current is suppressed drastically (Fig. 7). The nanolaminated layer has lower backward tunneling current (similar to pure Al_2O_3 film) and it can be easily erased than that of pure HfO_2 film (Fig. 7). The nanolaminated charge trapping layers can be operated up to large gate voltage (~20V). The nanolaminated memory devices have similar retention with pure Al_2O_3 memory devices (Fig. 8). The retention performance of HfAlO layer is degraded and it may be due to some unwanted defects in the film. An excellent retention is observed on 10 years projection for nano2 memory devices, as compared with all other memory devices (Fig. 9). A large memory window is found to be ~3.2V after 10 years retention. The HfO_2/HfAlO/HfO_2 memory devices have similar charge loss (~20%) with pure Al_2O_3 memory devices (Fig. 10), due to the charge storage in layer-by-layer.

4. Conclusions

The HfO_2/Al_2O_3 nanolaminated charge trapping layers with Al_2O_3 as blocking oxide have excellent memory window with good retention characteristics than that of all other memory devices. Therefore, SiO_2/nanolaminated HfO_2/Al_2O_3 layers/Al_2O_3 structure paves a way in future high performance flash memory device applications.

References

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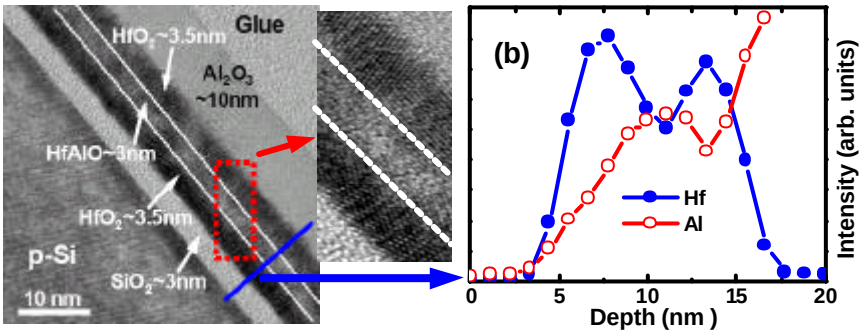

Fig. 1 (a) The cross-sectional TEM image of HfO_2/HfAlO/HfO_2 nanolaminated charge trapping layers with Al_2O_3 as a blocking oxide (sample: nano2), and a ~3-nm thick SiO_2 is used nominally. (b) The line profile of Hf and Al atoms by energy dispersive x-ray spectroscopy (EDS) measurement shows a clear HfO_2/HfAlO/HfO_2 structure.

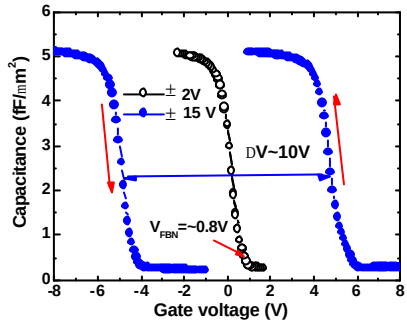

Fig. 2 A large counter-clockwise C-V (1MHz) hysteresis memory window is observed for HfO_2/HfAlO/HfO_2 structure with Pt gate. The ramp rate was 0.1V/s during C-V measurement.

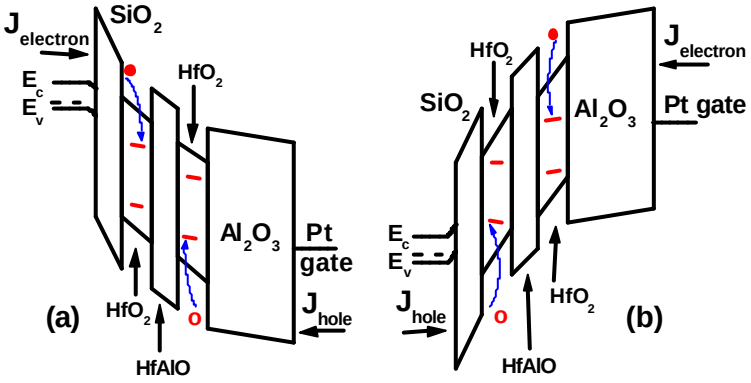

Fig. 3 A schematic energy band diagram of Al_2O_3 as blocking oxide on HfO_2/HfAlO/HfO_2 nanolaminated layers with SiO_2 as a tunneling oxide is shown under the devices (a) program mode and (b) erase mode. The high-κ Al_2O_3 as a blocking oxide is used to suppress the back tunneling current.

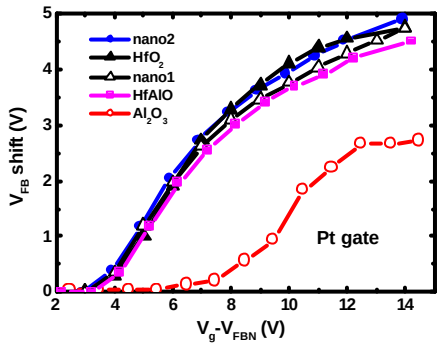

Fig. 4 Flat-band voltage (V_{FB}) shifts are calculated from C-V hysteresis of pure Al_2O_3 and HfO_2/Al_2O_3 nanolaminated charge trapping layers with Al_2O_3 as a blocking oxide.

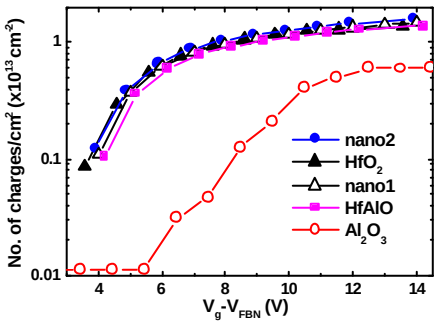

Fig. 5 The trapped charge densities in nanolaminated storage layers with Al_2O_3 as a blocking oxide are plotted. The charge storage density is calculated from C-V hysteresis curve (Fig. 4).

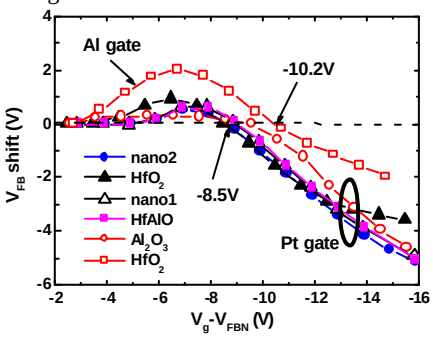

Fig. 6 Erasing characteristics of HfO_2/Al_2O_3 nanolaminated charge trapping layers. It is corroborating with the suppression of backward tunneling current in Fig. 7.

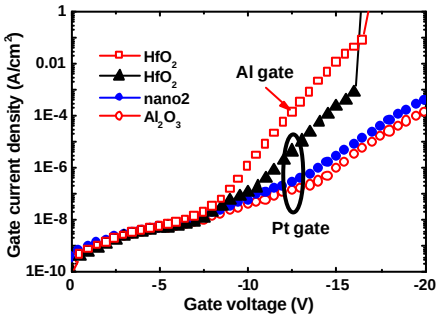

Fig. 7 The nanolaminated charge trapping layer has similar backward tunneling current as compared with pure Al_2O_3 layer at high field. At low field (>-8V), the gate leakage current for all memory devices are same. The back tunneling current can be suppressed using the high work function metal gate.

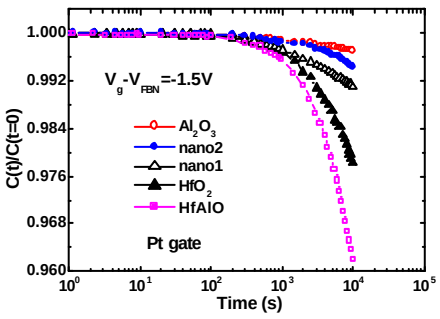

Fig. 8 Discharge characteristics of all memory devices are plotted. All charge trapping devices were stressed with V_g-V_{FBN}=6V, 60s before C-t measurement.

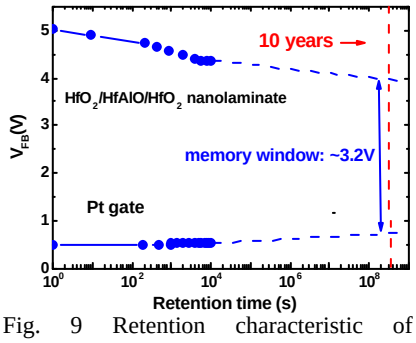

Fig. 9 Retention characteristic of HfO_2/HfAlO/HfO_2 double charge trapping layer (nano2). A large memory window (~3.2V) is observed after 10 years.

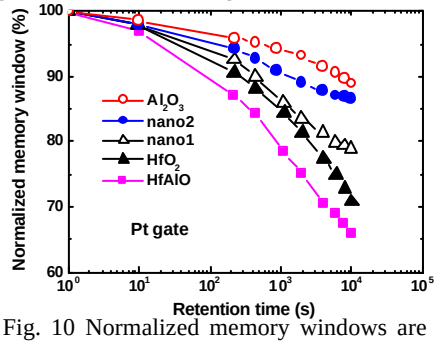

Fig. 10 Normalized memory windows are observed for all memory devices. The nanolaminated charge trapping layers have almost similar memory window with pure Al_2O_3 layers.