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Process Integration of Low-Power and High-Speed 16Mb MRAM using Multi-Layer Yoke Wiring Technology

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1. Abstract

High performance yoke wiring technology is developed for low-power and high speed 16Mb magnetoresistive random access memory (MRAM). The writing wiring is covered with conformal multi-layers of Ta/NiFe/Ta using a high ionization sputtering technique. This yoke wiring reduces the writing current by 60%, which is the most efficient ever reported. The 16Mb MRAM with 0.13 μm CMOS circuits is successfully demonstrated, showing low power consumption, high writing margin, high reliability and high yield.

2. Introduction

Recently, several studies have been reported for magnetoresistive access memory (MRAM), which features high density, low operation voltage, high speed, and long writing endurance[1][2][3][4][5] .

However, a large writing current is one of the most critical issues to realize high density MRAM. As the feature size decreases, the volume of free layer in the magnetic tunnel junction (MTJ) decreases, resulting in thermal instability as a non-volatile memory to guarantee ten year retention. To keep the thermal stability, the thickness of the free layer should be increased, which requires much higher magnetic field as the feature size decreases as shown in Fig. 1(a).

In this paper, high-performance yoke wiring technology is developed for 16Mb MRAM. The yoke wiring is fabricated by high ionization sputtering[6] and by a sophisticated process to efficiently concentrate a magnetic field on the MTJ and to drastically reduce the writing current. It demonstrates that highly stable operation of 0.13 μm 16Mb MRAM can be realized.

3. Issues and Actions

The key issues of yoke wiring technology in developing high density MRAMs are complicated processing, magnetic stray field and magnetic field variation caused by poor step coverage and poor sidewall grain growth control. The actions taken for these issues are also summarized in Fig. 2.

Simple Process

The process flow of our yoke wiring is shown in Fig. 3. To simplify the process, Cu damascene is used for the word line (WL), which is located under the MTJ. As sputtering step and a CMP step for the NiFe film are added to the conventional Cu damascene process. On the other hand, for the BL, which is located on the MTJ, Al wiring is used. It is difficult to cover the top and sidewall of the Cu damascene wiring with NiFe film by simple processing. Therefore, the process of sidewall spacer formation is utilized for Al BL wiring. The TEM photographs of the WL and the BL yoke wirings are shown in Fig. 4 (a) and (b), respectively.

Figure 5 shows the multi-layer structure of the yoke film. To prevent NiFe from out-diffusion to Cu, a Ta barrier is inserted between NiFe and Cu. To keep adhesion to the interlayer dielectric, a Ta adhesion layer is used. Consequently, a Ta/NiFe/Ta multi-layer is used for the yoke film.

The result of the stress induced void (SIV) test is shown in Fig. 6. It is found that no degradation due to the yoke wiring is observed after 400 hours stress at 200 ℃, which meets the specifications of wiring reliability as well as the conventional BEOL wiring.

Magnetic Stray Field Suppression

The yoke wiring acts as a parasitic bar magnet in the peripheral circuit. A line of magnetic force comes out from the magnetic N pole to S pole of the yoke wiring. As illustrated in Fig. 7, failing cells are observed at the array edge, because the magnetic stray field from the yoke wiring located at the peripheral circuit changes the switching field (H_c) of the array edge cells.

However, these failures disappear by using a thinner NiFe of 10 nm, because the remaining magnetic field is proportional to the thickness of NiFe.

Magnetic Field Variation Reduction

The step coverage of the yoke film drastically affects the switching characteristics of the MTJ with thin yoke wiring. When the sidewall of Al wiring has a side-etched shape, the yoke film is partially open as shown in Fig. 8. In this poor process, the WL and BL current margin map at the function test shows no writing window as shown in Fig. 8(b). On the other hand, an optimized process to suppress the Al side-etched shape leads to a large writing window as shown in Fig. 8(c), where the hatched area stands for no failure.

Figure 9 shows the relationship between the crystallinity and the switching field measured by a vibration sample magnetometer (VSM) for different sputtering angles of the conventional NiFe film. When the angle is large, some columnar grains are observed. The switching characteristics are degraded due to the remaining magnetic field caused by the columnar grains. To reduce the columnar grains, high ionization sputtering is utilized for NiFe deposition. The deposition model of the conventional sputtering and the high ionization sputtering are illustrated in Fig. 10 (a) and (b), respectively. The high ionization sputtering suppresses columnar grain growth and realizes excellent step coverage. It is verified that the yoke film deposited with high ionization sputtering shows no remaining magnetic field in the VSM (Fig.11) and shows much larger reduction of writing current compared with conventional sputtering (Fig. 12).

4. 16Mb MRAM

Asteroid curves with and without yoke wiring are shown in Fig. 13. The writing current is reduced by 60% using the yoke wiring designed in the previous sections.

The effect of the yoke wiring on the writing margin is investigated by comparing the following two samples. One has a 4 nm thick free layer without yoke wiring (sample (a)). The other has a 5.5 nm thick free layer with yoke wiring (sample (b)). Each writing margin is shown in Fig. 14. The latter shows a large writing margin to operate the 16Mb MRAM because of reduction in writing current and distribution. The standard deviation of writing current (σI_{SW}) is generally independent of the thickness of the free layer. In addition, σI_{SW} is reduced by the yoke wiring. Therefore, σI_{SW} of the sample (b) is smaller than that of the sample (a).

To guarantee data retention for ten years, the thickness of the free layer is determined to be 5.5 nm. By using the yoke wiring, the writing current is reduced, meeting the specifications of the 16Mb MRAM function.

A photograph of 16Mb MRAM and failure bit map are shown in Fig. 15. The 16Mb MRAM with the yoke wiring shows much less bit failures.

5. Conclusion

The yoke wiring has been developed using a simple process, stable multi-layer structure, and high ionization sputtering. The writing current is reduced by 60%. Finally, the functionality of 16Mb MRAM has been successfully demonstrated, showing a high writing margin, thermal stability and high reliability, and high yield.

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Reference

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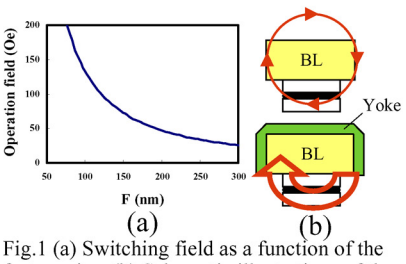

Fig.1 (a) Switching field as a function of the feature size. (b) Schematic illustrations of the magnetic field concentration effect of yoke

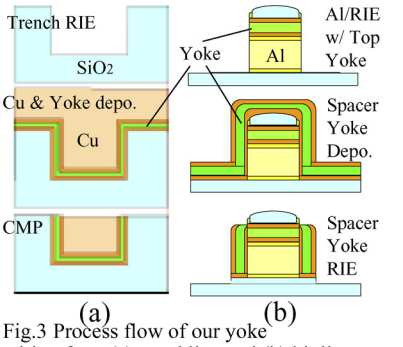

Fig.3 Process flow of our yoke wiring for a (a) word line and (b) bit line

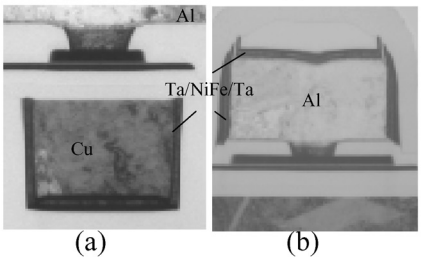

Fig.4 The cross-sectional TEM images of a (a) word line and (b) bit line with yoke.

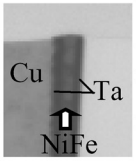

Fig.5 The enlargement of a word line yoke. Ta/NiFe/Ta multi-layer structure was formed for interface reaction prevention.

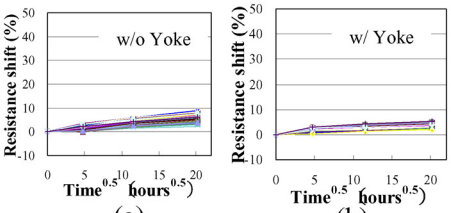

Fig.6 The stress induced void examination result of yoke wiring (a) and Cu wiring (b) respectively at 200 degree C. In yoke wiring, no resistance shift and good reliability results were obtained like Cu wiring.

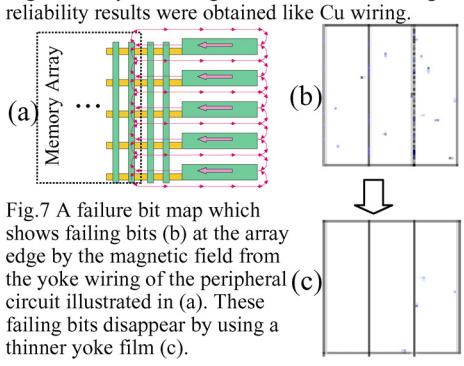

Fig.7 A failure bit map which shows failing bits (b) at the array edge by the magnetic field from the yoke wiring of the peripheral circuit illustrated in (a). These failing bits disappear by using a thinner yoke film (c).

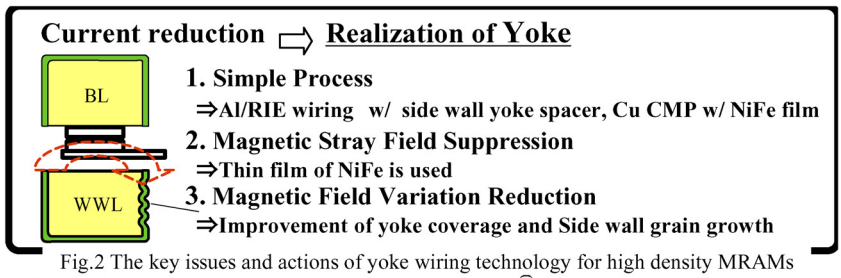

Fig.2 The key issues and actions of yoke wiring technology for high density MRAMs

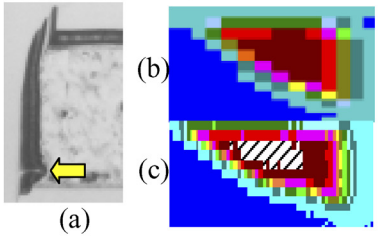

Fig.8 (a) The cross-sectional TEM image of a Bit line with a side-etched shape . The WL and BL current margin map are shown in (b) with the side-etched shape and in (c) after improving the side-etched shape. A hatched area of the map stands for no failures.

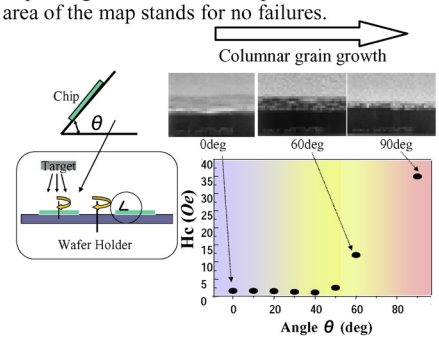

Fig. 9 Grain growth and the switching field (Hc) measured by a vibration sample magnetometer (VSM) for different sputtering angles of the conventional NiFe film.

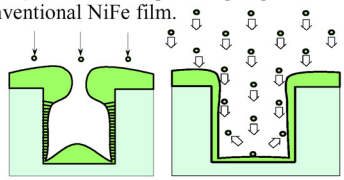

Fig.10 Schematic illustrations of the conventional process (a) and high ionization sputtering (b). High ionization sputtering suppresses columnar grain growth and realizes excellent step coverage.

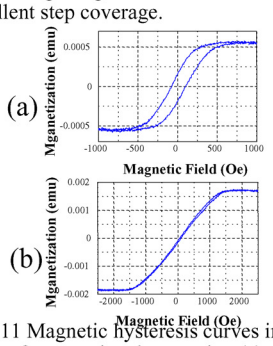

Fig.11 Magnetic hysteresis curves in the case of conventional sputtering (a) and high ionization sputtering (b). High ionization sputtering induces no remaining magnetic field .

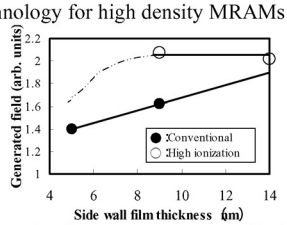

Fig.12 The ratio of current compares with the case of w/o yoke as a function of the sidewall film thickness in the case of high ionization sputtering and conventional sputtering respectively. The ratio of current increases by using high ionization sputtering.

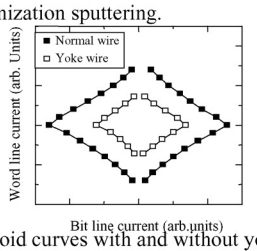

Fig.13 Asteroid curves with and without yoke wiring. 60% of the current can be reduced by the yoke.

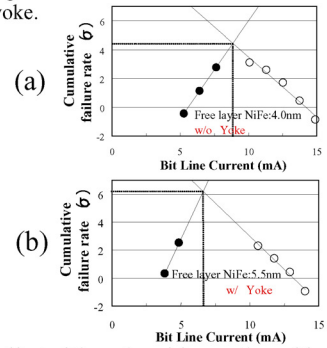

Fig.14 The effect of the yoke wiring on the writing margin. Sample (a) has a 4 nm thick free layer without yoke wiring. Sample (b) has a 5.5 nm thick free layer with yoke wiring. A closed circle stands for the selected state, that is, both WL and BL are selected. An open circle stands for a half-selected state, that is, only BL is selected. Sample (b) shows a large enough writing margin (more than 6σ).

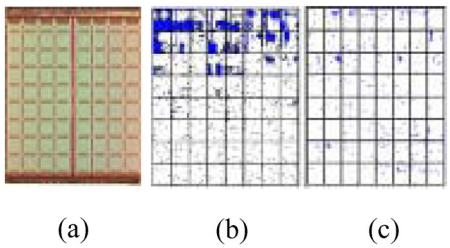

Fig.15 Photograph of the chip image of 16Mb MRAM (a). Failure bit maps of a 16Mbit without (b) and with the yoke wiring (c). By using the yoke wiring, the number of failing bits decreases drastically because of reduction in writing current.