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New Magnetic Nano-Dot Memory with FePt Nano-Dots

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1. Introduction

Demands for high density and high performance non-volatile memories have rapidly grown as the global market for mobile electronic devices expands in ubiquitous society [1]. Various kinds of non-volatile memories have been proposed and investigated. Flash memory is the most widely used non-volatile memory because it has several advantages such as high density, low manufacturing cost, stable operation, and so on. In recent years, however, flash memories face a serious problem concerned with a trade-off between reliability of charge retention and scaling down of tunneling oxide film thickness [2]. In order to solve this problem, we proposed a new non-volatile memory with high-density magnetic nano-dots (MND) dispersed in an insulating film as a floating gate. We call this new non-volatile memory "MND memory". In this study, we investigate the magnetic characteristics of MND formed by a novel self-assembled nano-dot (SAND) method. We also investigated the fundamental electrical properties for this new MND memory.

2. Basics of MND memory

Figure 1 schematically shows a cross-sectional structure of a memory cell and the operation principle of MND memory. As is obvious in the figure, one-transistor-type memory cell is used in the MND memory. The MND layer was formed between the blocking oxide and tunneling oxide, where each MND acts as a small floating gate. Furthermore, MND, tunneling oxide, and magnetic control gate compose a magnetic tunneling diode (MTD). The magnetic control gate made of a ferromagnetic material acts as a free layer for magnetic writing, whereas, MND acts as a pinned layer electrode because the MND requires a very high magnetic switching field due to the extremely small size. While the tunneling probability is high when the magnetic polarization for both free layer and pinned layer is parallel, the probability is low when the polarization for them is anti-parallel. The parallel polarization is preserved in the programming and erasing modes, and the anti-parallel polarization is preserved in the retention mode. The switching magnetic field to change the polarization, parallel or anti-parallel, is produced by flowing current through both a bit line (BL) and a word line (WL). In the programming mode, a negative voltage is applied to the control gate to inject electrons from free layer into the MND while the source or drain is maintained at the ground potential. In the erasing mode, a positive voltage is applied to the control gate through the WL with holding source and drain at the ground potential in order to emit electrons from the MND. In the programming and erasing modes, the magnetic polarization was parallel. After programming, magnetic polarization was changed to antiparallel polarization, which leads to low tunneling probability between control gate and MND. Excellent retention characteristics are expected even if extremely thin tunneling oxide is used because low tunneling probability prevents the charged electron leakage. Consequently, high speed programming and erasing can be achieved in this new MND memory with maintaining the advantage of high capability for scaling-down the memory cell size.

3. Experimental Results and Discussion

Figure 2 shows high-resolution transmission electron microscopy (HRTEM) cross-sectional images of as-deposited FePt-SiO_2 films formed by SAND method, where FePt and SiO_2 were co-sputtered using high-vacuum RF magnetron sputtering equipment. The FePt composition was defined as a ratio of area of FePt pellets to surface area of a SiO_2 target where the FePt pellets are placed. The sizes of FePt nano-dots with the FePt composition of 12%, 10%, and 8% were 3.5-4.5 nm, 2.5-3.5 nm, and 0.9-1.2nm, respectively. Moreover, the density of FePt nano-dots with the FePt composition of 12%, 10%, and 8% were 8.5×10^{12}/cm^2, 9.5×10^{12}/cm^2, and 2.5×10^{13}/cm^2, respectively. This indicated that the dot size and density were well controlled by the FePt composition. As-deposited FePt nano-dots were self-assembled into chemically disordered face centered cubic (fcc) phase. Thermal annealing can convert the chemically disordered FePt nano-dots into chemically ordered face centered tetragonal (fct) ferromagnetic FePt nano-dots. Figure 3 shows HRTEM cross-sectional image of FePt-SiO_2 film with the size ranging from 3.5 to 4.5nm after annealed at 600℃ for 1hour. As is clearly shown in Figure 3 (a), the size and density are not varied at all by the annealing. Figure 3 (b) also indicates that, after annealing at 600℃ for 1hour, the phase of FePt nano-dots converts into the fct phase. It is confirmed that the FePt nano-dots formed by SAND method were thermally stable. Figure 4 shows temperature dependence of coercivity (H_c) on FePt-SiO_2 film after annealed at 600℃ for 1hour measured by using a superconducting quantum interface device (SQUID). The H_c of FePt nano-dots measured at 293K, 100K, and 10K, were 1.15T, 1.75T, and 2.15T, respectively. By fitting the measured data to Sharrok's formula, we obtained the magnetocrystalline anisotropy (K_u) value of approximately 8.7×10^7 erg/cm^3. Figure 5 shows atomic force microscopy (AFM) results of FePt nano-dots films formed on a thermally oxidized silicon substrate. The thickness of the thermal SiO_2

thermal SiO_2 and the MND film were 10 nm and 10 nm, respectively. The surface roughness of Ra is 0.079 nm for as-deposited sample and 0.064 nm for the sample after annealing at 600℃ for 1 hour. Figure 6 shows the *C-V* characteristics of magnetic MOS capacitor with 10-nm- thick FePt-MND floating gate and NiFe control gate. The magnetic MOS capacitor consists of silicon substrate, thermal SiO_2 (10 nm), Al-O (3 nm), and NiFe (20 nm). The area size of capacitor gate is 1.5 μm ×6 μm. Lots of capacitors with the small gate area were connected each other to obtain a larger capacitance value. The total capacitor gate area is 100 μm× 100 μm. Hysteresis loops were observed, where the flat band voltage shifted from 0.4 V to 0.9 V. The hysteresises were caused by electron charging and discharging in the FePt MND floating gate. The clockwise direction of the *C-V* curve indicated that the charging and discharging of electrons occur between the floating gate and the NiFe control gate. Negative voltage is applied to the NiFe control gate in order to transfer the electrons from the NiFe control gate into the floating gate. As is clear in Fig. 6, the flat-band-voltage window was changed by the magnetic polarity after applying magnetic field, indicating that magnetic tunneling effect occurs between the MND floating gate and NiFe control gate.

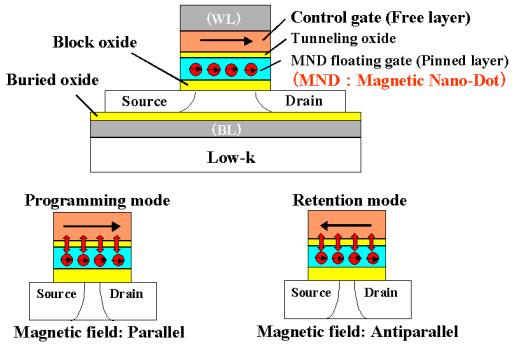

Figure 1. Cross-sectional structure and operating principle of MND memory.

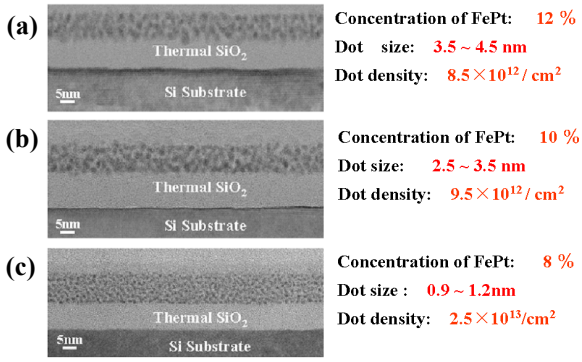

Figure 2. HRTEM cross-sectional images of 10-nm-thick FePt MND film formed on thermally oxidized silicon substrate: (a) FePt composition of 12%, (b) FePt composition of 10%, (c) FePt composition of 8%.

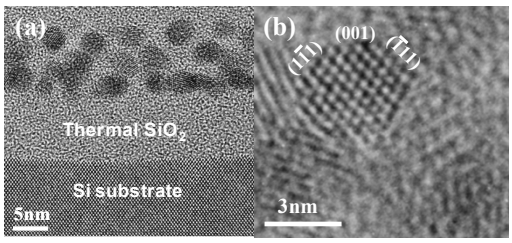

Figure 3. (a) HRTEM cross-sectional images of FePt MND film after annealing at 600℃ for 1hour. (b) Enlarged image of FePt nano-dot after annealing at 600℃ for 1hour.

4. Conclusions

High-density FePt nano-dots dispersed SiO_2 films were formed by using SAND method. After annealing at 600℃ for 1 hour, the FePt MND shows a high coercivity, which means that the FePt MND acts as a pinned layer. From *C-V* measurement, it was confirmed that the fundamental characteristics of magnetic MOS capacitor with FePt-MND floating gate were successfully implemented.

Acknowledgment

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References

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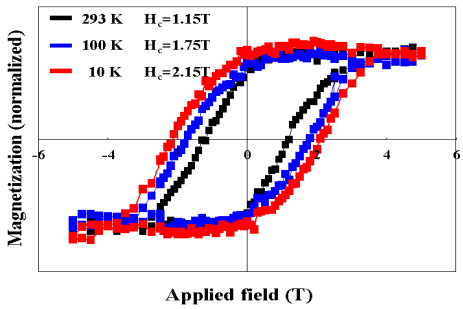

Figure 4. Temperature dependence of coercivity (H_c) on the FePt nano-dots film annealed at 600℃ for 1hour measured by SQUID.

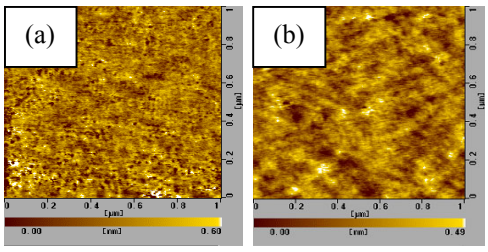

Figure 5. AFM result of FePt nano-dots film which formed on a silicon substrate with 10nm SiO_2 on its surface. (a) before and (b) after annealing at 600℃ for 1hour.

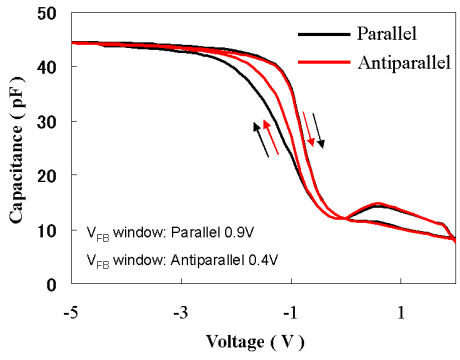

Figure 6. *C-V* characteristics of arrayed magnetic MOS capacitor.