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Optimization of Ring Type Electrode Process for High Density PRAM

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1. Introduction

In recent years, phase-change random access memory (PRAM) has been investigated as one of promising memories because of its non-volatility, relatively high endurance, and good scalability. It was reported that 256 Mb PRAM was successfully developed by adopting ring type bottom electrode contact (BEC) scheme and conventional 0.10 μm CMOS technology [1]. For high density PRAM products, it is very important to maintain stable cell uniformity for reliable operation since the writing current is mainly governed by the BEC size which is very sensitive to small process variation. In order to accomplish low writing current with uniform cell distribution, advanced storage module technology using ring type BEC was proposed. [2]

In malfunctioned chip with the ring-type contact, however, it is found that fail bits were originated from the recess of BEC area. In this work, it is shown that the recess can be eliminated using advanced ring type technology integrated with optimal core dielectrics as well as proper cell contact planarization process. Using this advanced ring type technology, it was possible to achieve flat and uniform BEC, which results in a wide sensing margin and high manufacturability.

2. Advanced Ring Type Contact Scheme

The formation of the ring-type contact based on 2-step chemical mechanical planarization (CMP) is schematically explained in Figure 1. At first, very thin TiN films were deposited inside the contact hole, which was followed by preparing core dielectrics on the TiN films. The uniform substrate was then prepared by metal CMP method, which generates final ring type bottom electrode.

Figure 2 shows the distribution of set and reset resistances for well-functioned and malfunctioned chips, respectively. In the malfunctioned chips, the tailing of reset resistance reduced the sensing margin. The fail bits show that the core dielectrics were severely recessed inside the ring type contact hole as the inset picture of TEM. The control of the recess amount is the key process to introduce the ring type BEC process into high density PRAM.

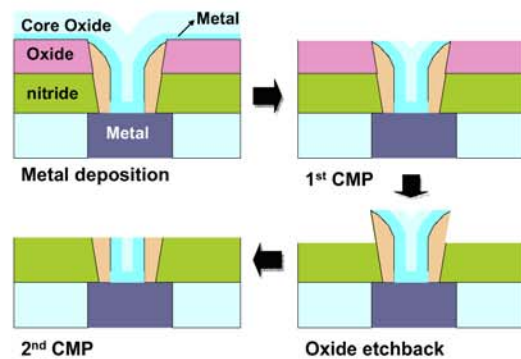


Figure 1: Schematic process sequences of ring-type BEC.

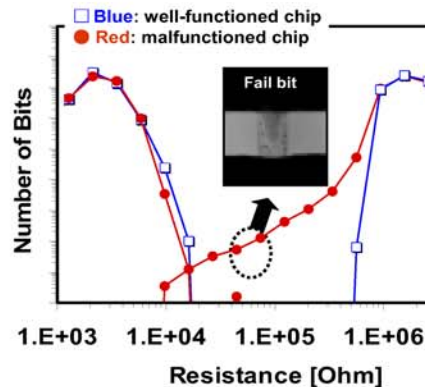


Figure 2: Resistance distributions of well-functioned and malfunctioned chips, and TEM analysis for fail bits.

In order to estimate the effect of the amount of the recess in the BEC, the result of the calculation of contact area with recessed BEC structure was shown in Figure 3. It was expected that the BEC contact area increased rapidly as a function of the amount of recess. In case the amount of recess in the ring type contact is above 100 \AA , the contact area is larger than that in normal pillar type. The recess amount have to be controlled within less than 100 \AA to advantage from the ring type BEC rather than the normal pillar type BEC.

It was found that very flat and uniform contact was fabricated using this advanced ring type structure while the recessed BEC was formed in conventional ring-type

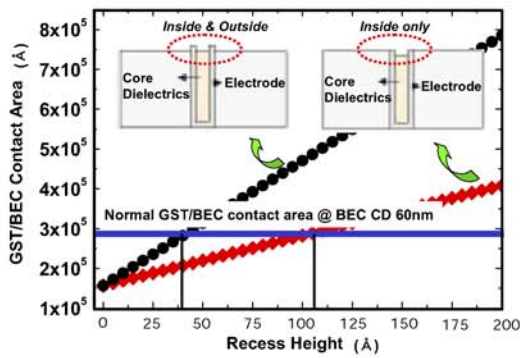


Figure 3: Calculated GST/BEC contact area as a function of recess height.

contact scheme. Figure 4 shows the TEM pictures of the cross-section and SEM images of surface of the sample to which we adapted recess-free ring contact schemes with optimized core dielectrics, wet cleaning and planarization process. We expect once such process optimization along with the development of advanced BEC process for precise transitional mechanism without reliability degradation such as neck broken, advancement of high-density PRAM with good reliability characteristics will be further accelerated.

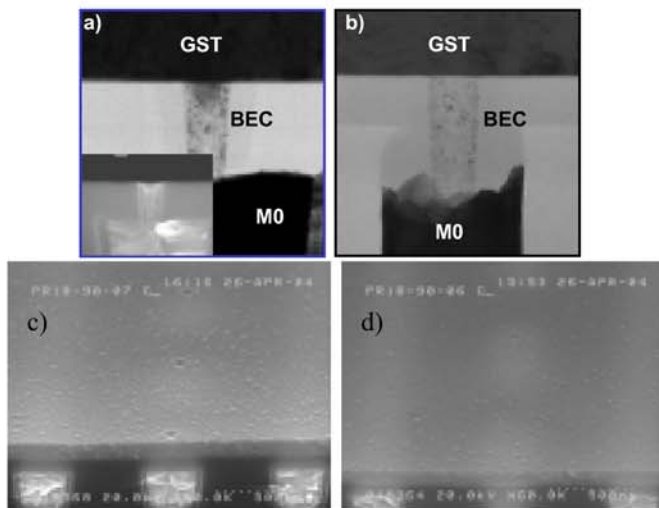


Figure 4: a), b) Vertical view and c), d) tilted view of recessed ring type contact and recess-free ring contact, respectively

It was found that the recess of core dielectrics in ring type structure results from the removal of core dielectrics in wet cleaning solution of CMP process. In our previous study, as BEC core recess is increased, reset current is also increased. So, optimizing the process to control recess rate is the key factor to reduce reset current without any reliability degradation. Thus, it is highly required to develop optimal core dielectrics and wet cleaning solution for the prevention of the recess. In addition to the optimal dielectrics and wet cleaning solution, the cell contact CMP process should be adjusted for the recess-free ring type contact. We have been able to significantly control BEC contact recess by new etching BEC and depositing new core material such as silicon nitride. And through a new process, better uniform interface was accomplished where phase transition occurs.

Figure 5 (a) shows the transition curves (R-I curves) of conventional and advanced ring type schemes, respectively. It was observed that the writing current was greatly reduced down to 0.45 mA using the advanced ring type structure, while the set resistance was increased to around 10kohms. Figure 5 (b) shows the writing current distribution of GST cells with normal ring type and recess-free ring type, respectively. In addition to the reduction in writing current, the distribution of writing current was greatly improved in the recess-free ring type contact

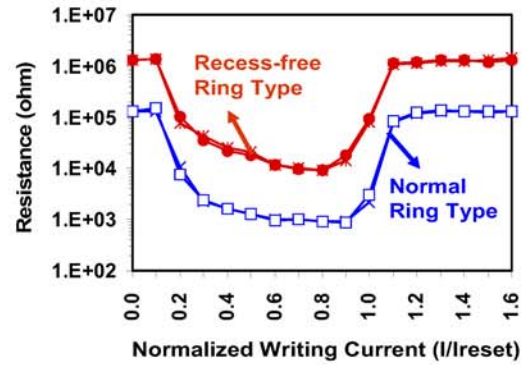
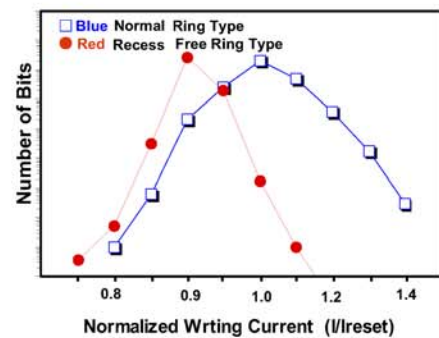


Figure 6: (a) Transition curves of GST cells with normal ring type and recess-free ring type.



(b) Writing current distribution of GST cells with normal ring type and recess-free ring type

3. Summary

An advanced ring type BEC process was successfully optimized for reliable high-density 256 Mb PRAM. This advanced ring-type BEC was prepared by the optimization of core dielectric, wet cleaning solution, and CMP process eliminating undesired recess issue in conventional ring type structure. Thus, it has been clearly demonstrated that the use of these advanced ring-type contact for high-density 512 Mb PRAM and beyond.

References:

- [1] S.J. Ahn *et al.* "Highly Reliable 50nm Contact Cell Technology for 256Mb PRAM," *Proceedings of VLSI*, 2005.
- [2] C. W. Jeoung *et al.*, "Highly Reliable Ring-Type Contact for High-Density Phase Change Memory", *Jpn. J. Appl. Phys.* **45** (2006) 3233