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Characteristics Improvement of Phase Change Memory with Programming Pulse Width

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1. Introduction

Owing to the distinctive features associated with nonvolatility, high speed, low power, scalability, and low cost, Phase Change Memory (PCM) has been considered as the most promising alternative for the next generation of nonvolatile semiconductor memory. Basically, PCM is based on the fast and reversible phase transitions between amorphous and crystalline phases of chalcogenide materials, which are thermally induced by Joule heating of current pulse, to compose two binary memory states corresponding to high resistive RESET state and low resistive SET state, respectively. Despite the great potential of PCM technology, the high programming current is still a limitation in downsizing the unit area of PCM cell. Some innovative methods inclusive of novel structures [1-3] or new materials [4-5] have been proposed to effectively reduce the programming current. However, one common drawback with these methods is that the SET resistance can not be programmed low enough so that some unwanted effects like the small sensing margin, poor uniformity, or short endurance degrade the device performance. One way to solve this is to prolong the programming pulse width so as to provide enough crystallization time to achieve lower SET resistance. In order to understand the pulse width effect on PCM devices in depth, this work gives a complete exploration of device characteristics concerning the RESET and SET pulse width.

2. Process Integration and Measurement Setup

In this work, a 0.18 μm CMOS back-end-of-line (BEOL) process was used to fabricate the PCM device with T-shaped structure as shown in Fig. 1. As can be seen, the $Ge_2Sb_2Te_5$ (GST) film with TiW top electrode (TE) is sputtered and stacked on the tungsten plug with a diameter of 0.24 μm. Although the programming current of these devices is too high due to the large contact area between GST and heater, some basic device characteristics can be still obtained as a good reference for smaller size devices. The schematic view of the measurement setup and programming strategy used to evaluate the device characteristics in this work are illustrated in Fig. 2.

3. Results and Discussion

Fig. 3 shows the measured I-V curves for the amorphous and crystalline states with the voltage pulse of 100 ns. An obvious threshold switching occurs at about 0.8 V and two low field states can be also clearly recognized. Fig. 4 shows the amorphous state I-V curves as a function of pulse width. In particular, the threshold voltage is slightly related to the pulse width.

From the relation between reading resistance and programming voltage (R-V), the PCM device characteristics can be evaluated. By programming the devices to nearly the same amorphous state, the reading resistance as a function of programming voltage pulse amplitude and width is shown in Fig. 5. As revealed by the figure, the SET resistance is clearly reduced as the pulse width increases so that the sensing margin (defined as R_{reset}/R_{set}), which is mainly determined by the SET resistance, is improved. Fig. 6 also summarizes the estimated SET resistance and sensing margin as a function of programming pulse width. The higher SET resistance resulting from shorter pulse also implies that a partially crystalline state formed during the SET programming.

Fig. 7 shows the microscopic morphology analyzed by the cross-sectional TEM for the PCM device programmed with a short SET pulse of 50 ns. Some fine grains are apparently distributed in the active region, but the amorphous phase still remains in the regions near the tungsten plug. It is speculated that the partially crystalline state is one of the reasons to cause the poor uniformity and endurance. The other case, as shown in Fig. 8, is with an extremely long SET pulse of 1 ms. The result clearly indicates that ultra large grains form in the chalcogenide film near the tungsten plug. These large grains have been further verified by the TEM nano-beam diffraction and dark field analysis. As a result, the crystalline characterization obtained from the TEM analysis makes a good agreement with the electrical performance as shown in Fig. 5.

Fig. 9 and 10 provide a comparison of device endurance performance between SET pulse widths of 100 ns and 1 ms. As has been demonstrated, the result for the short SET pulse reveals smaller sensing margin and the SET resistance tends to be gradually increasing with cycles and then a failure of RESET stuck appears after 10^6 cycles. On the other hand, the long pulse case provides a larger sensing margin and more stable SET resistance distribution. Moreover, it survives more than 10^7 cycles. The differences between these two cases may be attributed to the incomplete crystallization for short SET programming case.

4. Conclusions

Phase change memory cells were fabricated using a 0.18 μm BEOL CMOS process and the device characteristics concerning the pulse width were investigated in this work. The result provides a consistent correlation between electrical and morphological characterization to demonstrate the existence of partly crystallization in the PCM device when the SET pulse width is not long enough. Furthermore, it is found that incomplete SET programming is the major factor to degrade the PCM device performance, such as sensing margin, uniformity, and endurance. Therefore, an optimization in pulse width is necessary to improve the PCM device performance, especially for the smaller size devices developed in the future.

Acknowledgements

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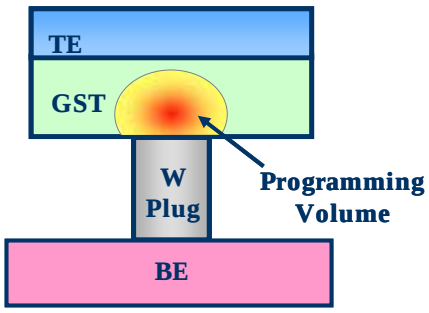
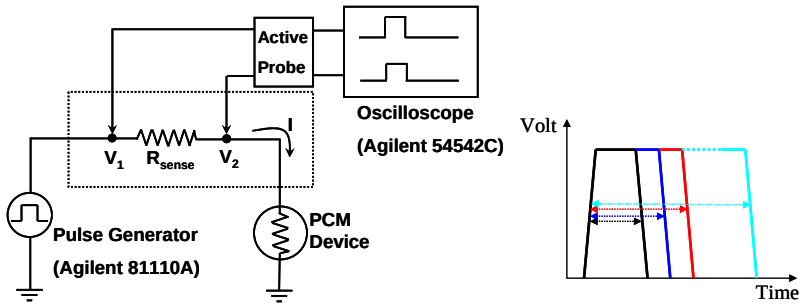


Fig. 1 Schematic cross section of PCM device with T-shaped structure



(a) (b)

Fig. 2 Schematic view of (a) measurement setup and (b) programming strategy used to evaluate the PCM devices

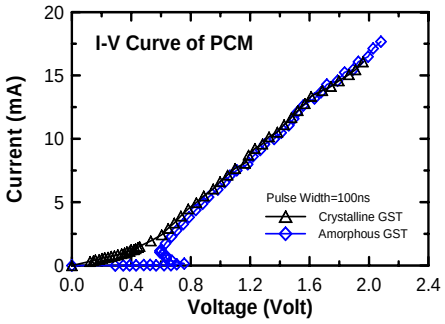


Fig. 3 Measured I-V curve of PCM device with the pulse width of 100 ns

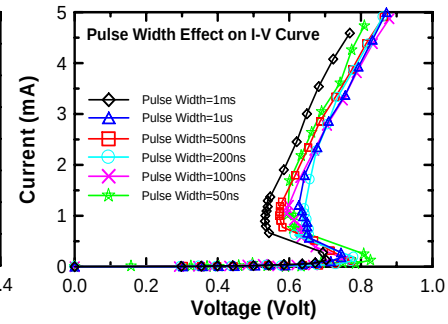


Fig. 4 Measured amorphous state I-V curves as a function of pulse width

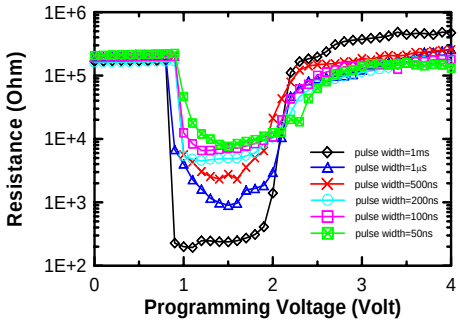


Fig. 5 Measured amorphous state R-V curves as a function of pulse width

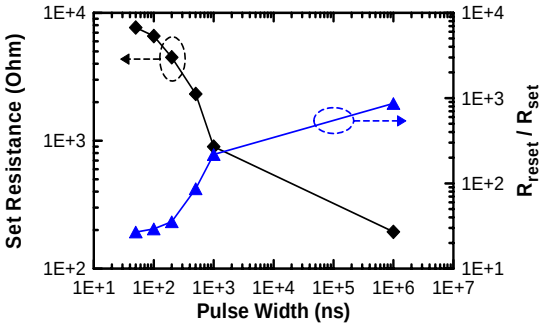


Fig. 6 Estimated SET resistance and sensing margin as a function of pulse width

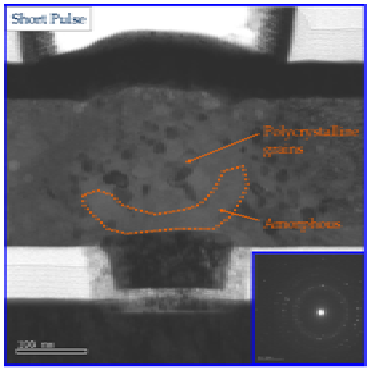


Fig. 7 TEM cross-sectional micrograph of PCM device programmed with a short SET pulse of 50 ns

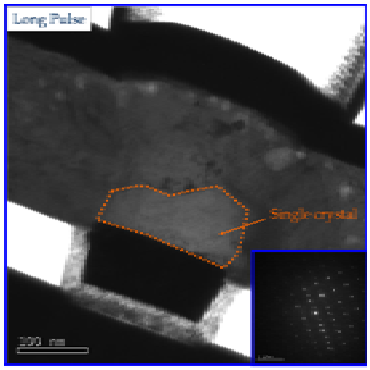


Fig. 8 TEM cross-sectional micrograph of PCM device programmed with a long SET pulse of 1 ms

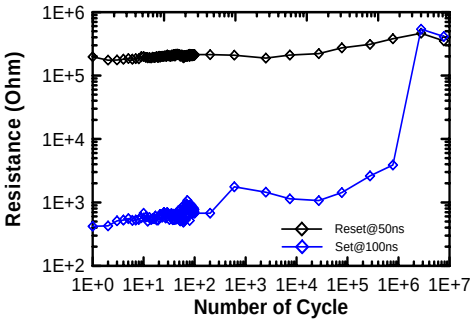


Fig. 9 Endurance performance of PCM device programmed with a short SET pulse of 100 ns

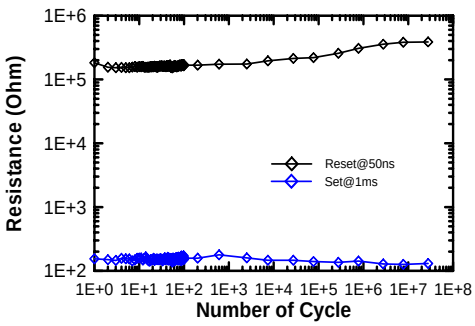


Fig. 10 Endurance performance of PCM device programmed with a long SET pulse of 1 ms