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Dopant Segregated Pt-Germanide Schottky S/D p-MOSFET with HfO_2/TaN gate on Strained Si-SiGe channel

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1. INTRODUCTION

CMOS scaling requires ultra-shallow source-drain junction which is currently limited by dopant activation and out-diffusion. Schottky barrier (SB) source-drain transistor is very appealing due to low thermal budget, low resistivity, atomically abrupt junction and high velocity overshoot at source [1]-[4]. However, the main difficulty in integrating Schottky S/D is finding the appropriate silicide with low Schottky barrier (SB) 0.06 ~ 0.1eV [3] or <0.3eV [7]. High SB results in low drive current and poor subthreshold behaviour. Recently, dopant segregated (DS) silicide has been introduced which greatly improve SB and make SB workfunction tunable [3]. At the same time, Ge channel devices with Pt germanide Schottky p-MOS have been demonstrated with high drive current due to a effective negative hole barrier, but suffer from high off-state leakage due to a negative SB [4],[12].

In this paper, we introduce a strained Si/SiGe channel coupled with dopant segregated SB source-drain. The compressive strain in SiGe layer results in significant reduction in its energy bandgap, making it possible to modulate the SB of PtSi/SiGe by the [Ge] concentration [5]. In addition, DS improves the off-state leakage and on-state drive current, while suppressing hot-carrier degradation.

2. EXPERIMENT

P-channel MOSFETs are fabricated on p-type Si substrate with 45Å HfO_2 gate dielectrics and 1000 Å TaN as gate electrode. Strained channel consisting of 50Å $Si_{1-x}Ge_x$ with x ranging from 10% to 30%, capped with 20 Å of Si were deposited in UHVCVD system at 4×10^{-6} Torr. **Fig. 1** shows the integration scheme of the PtSi Schottky source-drain p-MOSFET with strained Si/SiGe channel. Two different silicidation schemes were used: conventional silicidation of 300 Å Pt on exposed Si source-drain and dopant segregated (DS) Schottky SD using a pre-silicide implant of BF_2 (10 keV) followed by Pt silicidation. Silicidation is carried out at 500°C in N_2 ambient and excess un-reacted Pt is removed in aqua regia solution. Control samples with Si channel and strained $Si/SiGe_{0.2}$ channel with conventional SD p^+-n junction were also fabricated for comparison.

3. RESULTS AND DISCUSSIONS

Fig. 2 shows the transfer graph (I_d-V_g) for gate length L_g = 0.5 μm. DS SB transistor shows much higher drain current as compared to conventional SB transistor without DS. In addition, gate induced leakage current is also smaller for DS. **Table 1** summarized the key advantages of using DS together with SiGe channel. Lower hole barrier coupled with higher channel mobility can be achieved without sacrificing I_{on}-I_{off} ratio. The transistor performance in term of I_d-V_g, I_{on}-I_{off} ratio and drain-induced barrier lowering (DIBL) are described in **Figs. 3** to **5** for PtSi Schottky S/D p-MOSFET on strained $Si/SiGe_x$ channel compared to conventional p^+-n S/D junction transistors. Schottky S/D transistor tends to be better in terms of DIBL due to adrupt junction but suffers from low I_{on} due to high Φ_{Bp} (Fig. 4). However, this could be mitigated by dopant segregation (DS) (**Figs 4** and **8**).

Fig. 6 describes the mobility improvement when strained $Si/SiGe_x$ (x =20%) is used as compared to control Si channel. Significant mobility improvement of up to 1.5X is observed at low field (E_{eff} = 0.4 MV/cm) for strained Si/SiGe p-MOSFET and additional mobility improvement (up to 2.5X) is further observed when DS PtSi for source-drain is used on strained Si/SiGe channel.

Figs. 7 to 9 describes the various aspects of Schottky barrier formed on strained $Si/SiGe_x$ (x ranging from 10% to 40%). Figs. 7 and 8 show that DS on strained Si/SiGe channel improved forward current significantly due to the lowering of hole barrier, Φ_{Bp} without affect the off-state leakage. The modulation of SB using different Ge % is also modified when DS scheme is used as shown in **Fig. 8**. Barrier lowering is significantly enhanced when DS is used in conjunction with strained Si/SiGe channel especially at low Ge concentration. **Fig. 10** shows the gate leakage for Schottky and junction SD which is comparable to reference data.

Fig. 11 and **12** shows the hot-carrier stressing on Schottky S/D p-MOSFET. DS tends to alleviate HCI for both maximum electron injection condition ($V_g = V_d$) and maximum substrate injection ($V_g = V_d/2$) which can be explained by lower effective field at drain due to higher low-field mobility [13].

4. CONCLUSION

Dopant segregated (DS) Schottky SD with strained Si/SiGe p-channel MOSFET is presented with high hole mobility, high drive current, and enhanced hot carrier immunity.

References [1] M. Nishisaka et al, *SSDM*, p. 586, 2002. [2] H. C. Lin et al, EDL, p. 102, 2003. [3] D. Connelly et al, EDL, p. 411, 2003. [4] A. Kinoshita et al, *VLSI Tech. Symp.*, p. 158, 2005. [5] R. Li et al, , *EDL*, 2006. [6] K. Ikeda, et al, *EDL*, p. 670, 2002. [7] J. Kedzierski et al, *IEDM Tech. Dig.*, p. 3.4.1, 2000. [8] M. Fritze et al, *EDL* ., p. 220, 2004 [9] H. Iwai, et al, Microelectronic Eng., p. 157, 2002. [10] B. Guillaumont et al, IEDM, p. 355, 2002. [11] O. Weber et al, IEEE TED, p. 449, 2006. [12] K. Ikeda, et al, EDL, p. 670, 2002. [13] D. Onsongo et al, TED, p. 2193, 2004.

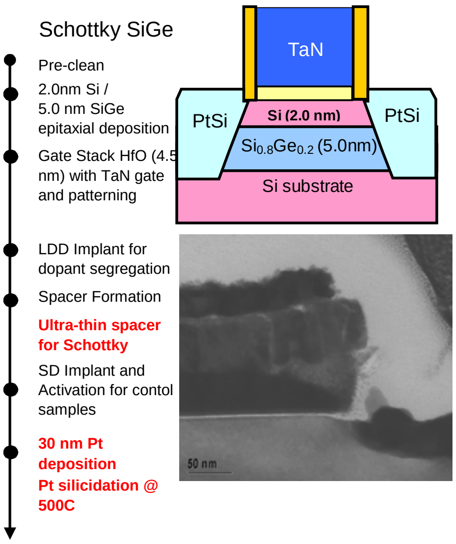

Fig. 1 Integration scheme of strained Si/SiGe channel with ultra-thin spacer and Pt silicide Schottky barrier for source-drain. Inset shows the TEM of the structures.

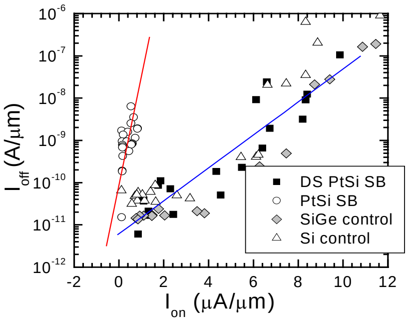

Fig. 4 I_{ON}-I_{Off} chart for samples with DS-Schottky and PtSi Schottky SD on strained Si/SiGe$_{0.2}$ as compared to control Si and strained Si/SiGe$_{0.2}$ channel samples with conventional SD junction.

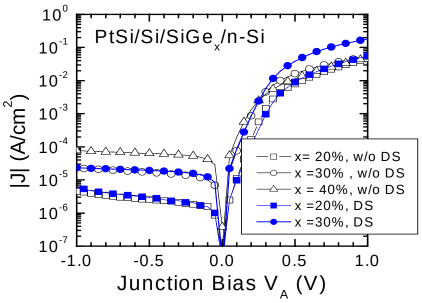

Fig. 7 Junction leakage for different Si/SiGe$_x$ with x ranging from 20% to 40% with and without DS Schottky barrier junction. DS increases the forward current without affecting the reverse bias leakage.

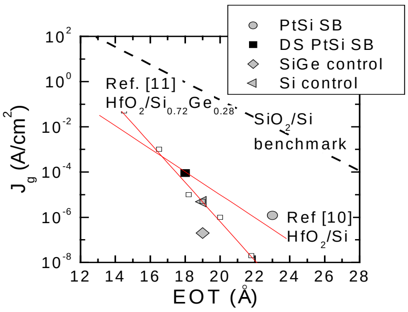

Fig. 10 Gate leakage versus EOT for different channel, Si, Strained SiGe$_{0.2}$ with HfO$_2$ and TaN gate, with Schottky and junction (control) SD.

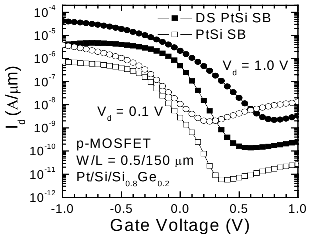

Fig. 2 I_d-V_g characteristics of p-MOSFET with strained Si/SiGe$_{0.2}$ and Schottky barrier SD using PtSi with and without DS.

	$\Phi_{B,hole}$ (eV)	I_{ON}-I_{OFF} @ V_d = -0.1V	EOT (Å)	$\mu_{p,eff}$ @ 1MV/cm (cm^2/V-S)	References (Year)
Pt-Ge sub	-0.1	~ 10^4	HfO$_2$ (29 Å)		[5], 2006
Pt-Si on SOI	0.22	> 10^5	SiO$_2$ (40 Å)		[7], 2000
Pt-Si (Bulk)	0.23	> 10^4	SiO$_2$ (18 Å)		[8], 2004 [9], 2002
P+ SiGe$_{0.28}$	NA	> 10^2	HfO$_2$ (16.5 Å)	90	[11], 2006
DS CoSi$_2$ on Si (Bulk) with Deep II		10^{-4} (Vd = 2V) 10^7 (V_d = 2V)	SiO$_2$ (25 Å)	50	[4], 2005
DS Pt-SiGe$_{0.2}$	0.18 ~ 0.12	10^6	HfO$_2$ (18 Å)	148	This work

Table 1 : Summary of different transistor parameters for Schottky SD transistor with different silicidation scheme and channel

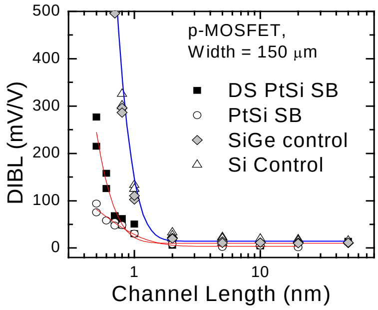

Fig. 5 DIBL versus channel length for PtSi Schottky SD p-MOS with and without DS. Also shown are Si and SiGe control. DIBL is high as channel is un-implanted.

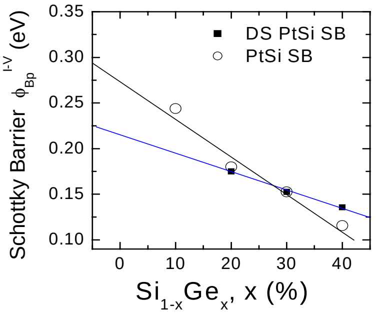

Fig. 8 Thermonic hole SB calculated using I-V methods for different Ge percentage in SiGe layer. Bandgap in SiGe is calculated using $E_{g,SiGe_x} = E_{g,Si} - 0.9x + 0.4x^2 - 0.13x^3$

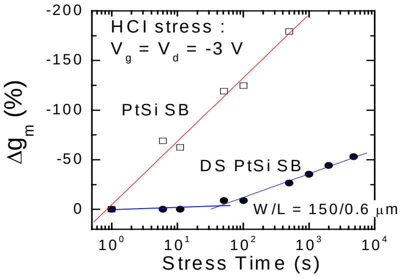

Fig. 11 HCI (V_g = V_d = -3V) stressing on strained Si/SiGe$_{0.2}$ with Schottky SD with and without DS

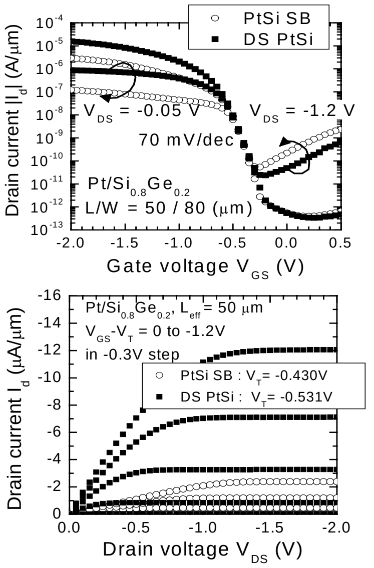

Fig. 3 I_d-V_g and I_d-V_d for long channel p-MOSFET with strained Si/Si$_{0.8}$Ge$_{0.2}$ channel and Schottky SD with and without dopant segregation. Very high subthreshold slope of 70 mV/dec are obtained.

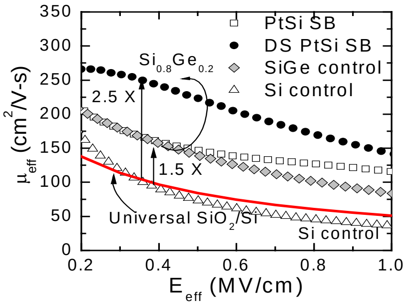

Fig. 6 Hole mobility for strained Si/Si$_{0.8}$Ge$_{0.2}$ p-MOS with Schottky S/D and SiGe control with p+-n SD junction. Close to 1.5X increase in hole mobility is observed with strained Si/Si$_{0.8}$Ge$_{0.2}$ and up to 2.5X increase with DS S/D

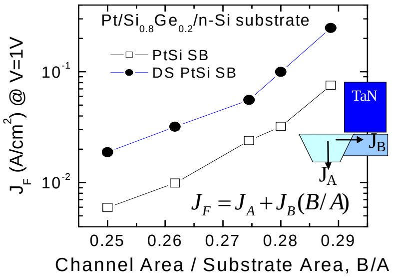

Fig. 9 Forward junction current density as function of the ratio between channel area and substrate area. B/A shows the ratio of current flowing through the PtSi/SiGe junction versus the PtSi/Si junction.

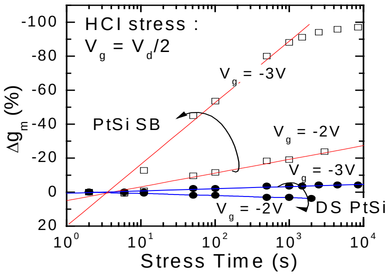

Fig. 12 Max I_{sub} HCI (V_g = V_d/2 = -2V, -3V) on strained Si/SiGe$_{0.2}$ p-MOS with Schottky SD