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Improved Performance of Schottky Barrier Source/Drain Transistors with High-K Gate Dielectrics by Adopting Recessed Channel and/or Buried Source/Drain Structures

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Abstract

In this paper it is shown that recessed channel structures are quite effective for improving cutoff characteristics and that buried source/drain structures are quite effective for increasing current drivability and suppressing electric field strength in gate dielectrics of Schottky barrier source/drain transistors with high-k gate dielectrics.

1. Introduction

The trend toward miniaturization has resulted in thinning of gate dielectrics and lowering of source/drain resistances, and according to the ITRS, they should be less than 1 nm and 150 Ωμm, respectively, within a few years. In order to avoid the drastic leakage current increase that is inherent in such thin SiO_2 gate dielectrics and to reduce source/drain resistances, high-k gate dielectrics and Schottky barrier source/drain transistors (SBT) are being intensively investigated [1, 2]. It was reported at the last SSDM that current drivability of SBT with high-k gate dielectrics is strongly degraded and that it is quite important to increase controllability of gate electrode over electrical potential at a substrate surface near a source/channel interface [3]. In the present work, we quantitatively investigated recessed channel structures in which a substrate surface near a source/channel interface is surrounded by a gate electrode from above and upper right from the viewpoint of current drivability and cutoff characteristics. Influences of buried source/drain structures on current drivability and electric field strength in gate dielectrics were also studied.

2. Model in Simulation

I_D-V_G characteristics at 300K were simulated at V_D = 0.7 V for 35 nm channel length nMISFETs having recessed channels and metallic sources and drains with x_j of 10 nm and ϕ_B of 0.2 eV (Fig. 1). Here, A and B are a depth of the recessed region and a distance between the recessed region and source/drain, respectively, and they are variables. We used an in-house 2-dimensional device simulator (DIAMOND) taking both thermal and tunneling current through Schottky junctions and barrier height lowering due to image charge into consideration [4]. The impurity concentration in the substrate was 1×10^{16} cm^{-3} at the substrate surface and 1×10^{18} cm^{-3} deep inside. A total equivalent oxide thickness (EOT) of a stacked gate dielectric was assumed to be 1 nm. A metallic gate electrode with an effective work function of 4.0 eV was assumed. Passivation layer was assumed to be SiO_2 (k = 3.9). V_{TH} adjustment was not carried out in this study.

3. Results and Discussion

In the case of a device with a recessed channel, electrical potential in the channel region is higher, i.e., Schottky barrier is thinner, even compared with a device with a single layer gate dielectric of k = 3.9 and a flat channel (Fig. 2). This phenomenon can be understood in terms of the fact that the substrate surface near the source/channel interface is surrounded by a gate electrode from above and upper right, resulting in an increase in capacitive coupling between gate and channel, C_{GC}, i.e., an increase in controllability of a gate electrode over electrical potential of the region. However, I_D of the device with a recessed channel is lower than that of the device with a single layer gate dielectric of k = 3.9 (Fig. 3). This phenomenon can be understood in terms of the fact that electrical current is prevented from flowing along the substrate surface, i.e., a current path is lengthened, in the case of the device with a recessed channel although electrical potential is the highest at the surface (Fig. 4). Hence, in devices with recessed channels, there is a trade-off between a large C_{GC} and a long current path resulting in a maximum around A = 4 nm and B = 1.5 nm (Fig. 5). It should be noted that both a large C_{GC} and a long current path are preferable for cutoff characteristics: the device with a recessed channel shows the best characteristics among the 4 devices (Fig. 6).

The thin Schottky barrier in the case of the devices with recessed channels (Fig. 2) implies a high electric field at the substrate surface near the source/channel interface. Hence, it is foreseen that high electric field is induced in gate dielectrics of devices with recessed channels around the source/channel interface, which is unfavorable from the viewpoint of reliability. In the case of devices with deep recessed channels, the electric field is quite high, around 15 MV/cm (Fig. 7). In order to suppress the electric field strength, devices with buried source/drain (Fig. 8) were studied. The structure is equivalent to that in Fig. 1 except for source/drain. Here, C is a buried depth of source/drain and it is a variable. Electric field strength rapidly decreases as a buried depth of source/drain increases (Fig. 9); it is lower than 6 MV/cm even in the case that the buried depth is only 1 nm. Hence, devices with buried source/drain are quite effective for suppression of electric field strength in gate dielectrics. However, it is foreseen that both cutoff characteristics and current drivability might be degraded by burying source/drain, because EOT is thicker than that of gate dielectrics due to the semiconductor layer above source/drain. We found that current drivability even increases in the case that the buried depth is shallow (Fig. 10), although S-factor increases, i.e., cutoff characteristics are degraded (Fig. 11). In the case of a device with a flat channel, the highest drain current is 792 μA/μm, which is more than twice that of the devices with a flat channel and without a buried source/drain. The high current drivability can be understood in terms of the fact that electrical current can flow out of not only side but also upper surface of source; in particular, it can flow out of the upper right corner of the source region to an arbitrary direction between upside and right in the case of devices with buried source/drain. The devices with buried source/drain have a trade-off between cutoff characteristics and current drivability. An XY-plot between I_D at $V_G = V_D = 0.7$ V and S-factor is shown in Fig. 12. It is known from this figure that flat channel devices can realize extremely high current drivability as compared with devices without a buried source/drain and that cutoff characteristics are quite effectively improved in devices with recessed channels.

4. Summary and Conclusion

It has been shown that recessed channel structures are quite effective for improving cutoff characteristics and

that buried source/drain structures are quite effective for realizing extremely high current drivability and reducing electric field strength in gate dielectrics. Designing device structure around channel and source/drain can improve electrical characteristics of devices with high-k gate dielectrics.

References

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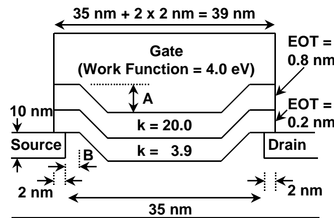

Fig. 1. Device structure with a recessed channel used in the simulations.

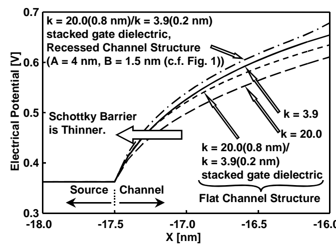

Fig. 2. Electrical potentials at the substrate surface near the source/channel interface in the device shown in Fig. 1 and those with flat channels at $V_G = V_D = 0.7$ V.

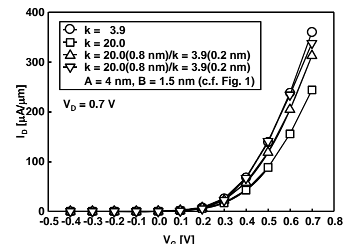

Fig. 3. I_D-V_G characteristics of the device shown in Fig. 1 and those with flat channels.

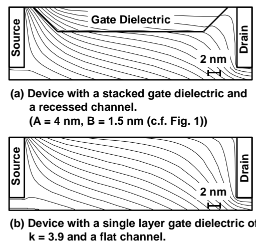

Fig. 4. Equipotential curves near substrate surfaces at $V_G = V_D = 0.7$ V.

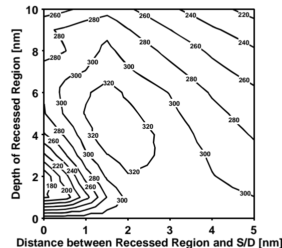

Fig. 5. Contour map of I_D (μA/μm) at $V_G = V_D = 0.7$ V.

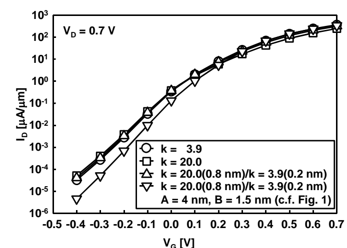

Fig. 6. I_D-V_G characteristics of the device shown in Fig. 1 and those with flat channels.

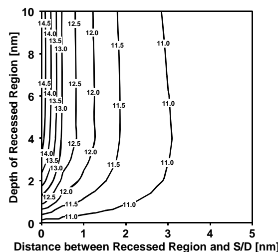

Fig. 7. Contour map of electric field strength in gate dielectrics (MV/cm) at the source/channel interface at $V_G = V_D = 0.7$ V.

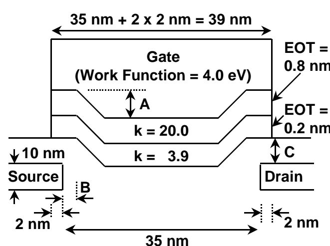

Fig. 8. Device structure with a recessed channel and a buried source/drain used in the simulations.

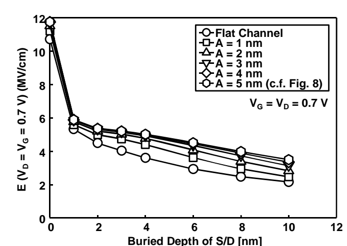

Fig. 9. Dependences of electric field strength in gate dielectrics at the source/channel interface on a buried depth of source/drain. Here, $V_G = V_D = 0.7$ V and B in Fig. 8 = 1.5 nm.

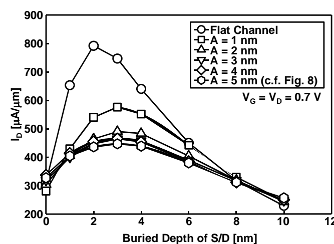

Fig. 10. Dependences of I_D on a buried depth of source/drain. Here, $V_G = V_D = 0.7$ V and B in Fig. 8 = 1.5 nm.

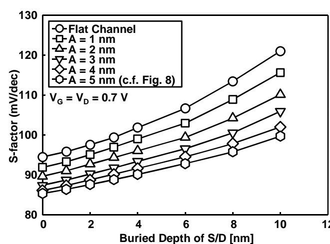

Fig. 11. Dependences of S-factor on a buried depth of source/drain. Here, $V_G = V_D = 0.7$ V and B in Fig. 8 = 1.5 nm.

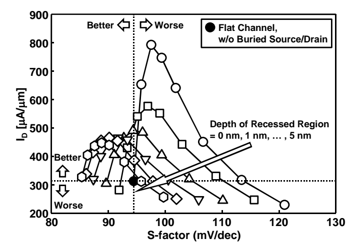

Fig. 12. Dependences of I_D at $V_G = V_D = 0.7$ V on S-factor. Here, a buried depth of source/drain is variable and B in Fig. 8 = 1.5 nm.