Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 1006-1007

F-9-3

Examination of Performance Improvement in Dopant Segregated Schottky MOSFETs; Short Channel Effects, Carrier Velocity and Parasitic Resistance

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Abstract

Performance improvement in dopant segregated Schottky (DSS) MOSFETs was examined experimentally. We investigated effective junction depth (x_j), carrier velocity and parasitic resistance (R_{para}) for DSS and conventional (conv.) FETs and found that these factors are improved in DSS FETs. We focus on the reduction of R_{para} and discuss the potentiality of DSS FETs as a candidate for future ULSI devices.

Introduction

Schottky source/drain MOSFETs have attracted much attention as a candidate for high-performance device in future ULSIs [1-5]. We have proposed a novel Schottky source/drain structure using the dopant-segregation (DS) technique in order to lower the effective barrier height φ_B (Fig.1), and the improvement in short channel effect (SCE) immunity and the enhancement of drive current by 20% in 50nm devices have been successfully demonstrated [6,7].

In this paper, we experimentally analyze the origins of performance improvement in *n*DSS FETs. From the viewpoint of SCE immunity, effective x_j in DSS junction is estimated. We also investigate the carrier velocity and R_{para} to study the drive current enhancement. We especially focus on R_{para} reduction and discuss the current drivability of DSS FETs as compared to conv. FETs.

Results and Discussions

A. DSS Junction Depth

To evaluate electrical x_j for DSS and conv. FETs, we measured gate edge junction capacitances (C_{GE}). In Fig. 2, C_{GE} for conv. FETs decreases faster than that for DSS FETs with increasing V_d. This is consistent with the fact that DIBL is well suppressed in DSS FETs [6]. It can be seen from Fig. 2 that C_{GE} for DSS is about 75% of that for conv. FETs. According to another measurement of junction capacitances per unit area (not shown), depletion layer width for DSS junction is about 65% of that for conv. junction. Hence it can be concluded that effective x_j for DSS FETs is about half as compared to conv. FETs. This certainly contributes to SCE immunity.

B. Carrier Velocity

It was shown that the electron-injection velocity through Schottky junction is higher than that of normal PN junction [4]. Figure 3 shows that impact ionization is enhanced by 20% in DSS FETs. This indicates that, even near the drain edge, the electron velocity is higher in DSS than in conv. FETs, which can be one of factors for the drive current improvement in DSS FETs.

C. Parasitic Resistance

To compare R_{para} between DSS and conv. FETs, we use the Terada's method [8] for R_{para} extraction. However, this method cannot be applied to the device with V_g -dependent R_{para} as shown in Fig. 4. In the present study, we simply choose the physical gate lengths (L_{poly}) as the *actual* channel lengths to minimize the magnitude of error in R_{para} extraction (Fig. 4(b)) because the halo regions at the channel edges work as V_g -dependent R_{para}. It was confirmed by simulation that our method is valid within the device structures used in this work.

It should be noted that R_{para} reaches its saturation at sufficiently high V_g, where V_g-dependent components such as spreading and overlap resistances (R_{spr} and R_{ov}) are saturated. In Fig. 5, we obtained saturation R_{para} of 192 and 264Ωμm for DSS and conv. FETs (L_{ofs}=6nm), respectively. It can be seen from Fig. 6 that R_{para} for DSS FETs has much weaker V_g dependence, as compared to that for conv. FETs, which indicates that the V_g-dependent components are very small in DSS FETs. This result is quite reasonable because there is no extension in DSS structure and hence neither R_{spr} nor R_{ov} can be main factors of R_{para} in principle.

The offset resistance, which is another component of R_{para}, can be reduced by shortening L_{ofs} as shown in Fig. 7. R_{para} for DSS FETs reaches 130Ωμm at L_{ofs}=0, which mainly results from contact resistance (R_{co}). Although a similar value of R_{co} (120Ωμm) is estimated for conv. FETs [9], it is expected that contact *resistivity* is much reduced by DS technique, because effective contact area for DSS FETs is restricted only to the gate edges and is much smaller than that for conv. FETs.

Reduction of R_{para} enhances the drive current by 15% for 50nm devices as shown in Fig. 8. It is speculated that, by optimizing R_{para} (simulated value for L_{ofs} = 0 in Fig. 7), our DSS FETs will provide drive current enhancement of larger than 50% in the 22 nm technology node generation.

Conclusion

It has been shown that the SCE immunity in DSS FETs originates from shallowness of DSS junction. The enhancement of drive current attributes to high carrier velocity and reduction of R_{para}. Especially, the reduction of R_{para} mainly contributes and enhances the drive current by 15% in 50nm devices. In conclusion, DSS FETs are promising for sub-50nm LSI devices.

Acknowledgement

We would like to thank Daisuke Hagishima for supports and discussions.

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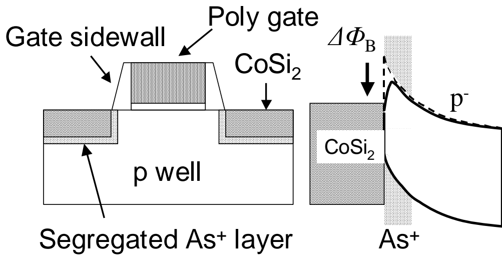


Fig.1 Schematic diagram of *n*DSS FET.

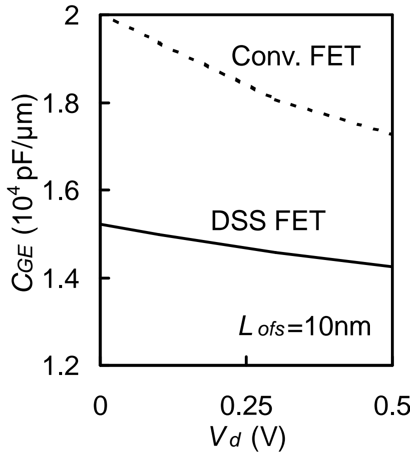


Fig.2 C_{GE} for DSS and conv. FETs as a function of V_d. The gate sidewall width (L_{ofs}) is 10nm for both FETs.

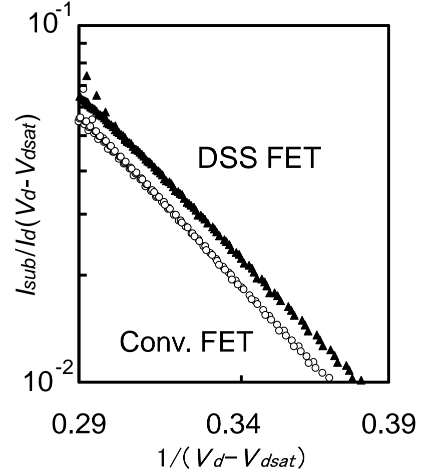
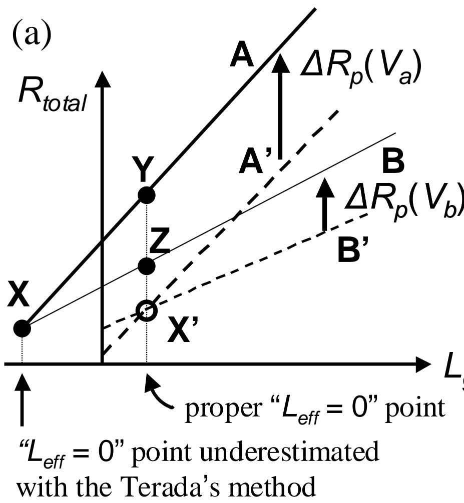


Fig.3 Plots of impact ionization rate for DSS and conv. MOSFETs.



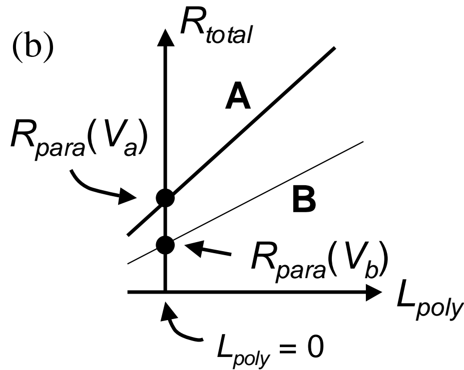


Fig.4 (a) Schematic illustration of the intrinsic problem of the Terada's method. In constant R_{para} case, the crossing point of two R_{total} -L_g lines (A' and B') at different gate overdrive V_{ov} =V_g-V_{th} (V_a and V_b) gives the correct R_{para} (X'). When V_g -dependent component ΔR_p is added to R_{para}, A' and B' shift differently and then the crossing point moves from X' to X. The Terada's method underestimates R_{para} at X, while proper R_{para}'s for A and B should be given by Y and Z, respectively. (b) R_{para} extraction method in the present study. R_{para} is obtained by extrapolating the R_{total}-L_{poly} plot to L_{poly} = 0.

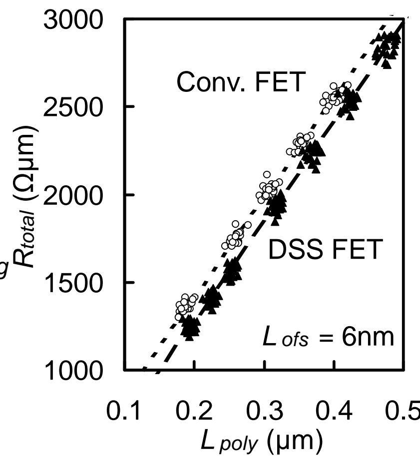


Fig.5 R_{total} - L_{poly} plots in the triode region (V_d=0.01V) for DSS (triangles) and conv. (open circles) FETs at the same effective V_{ov} (0.7V) where R_{para} is almost saturated. Broken and dotted lines are fitted lines.

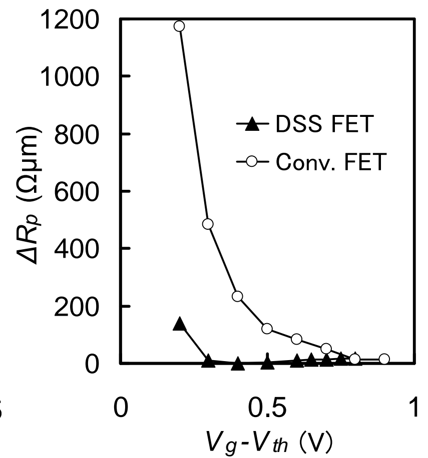


Fig. 6 V_{ov} (=V_g-V_{th}) dependence of ΔR_p = R_{para} - $R_{para\text{-}sat}$ for DSS and conv. FETs, where $R_{para\text{-}sat}$ is the saturation R_{para} at sufficiently large V_{ov}.

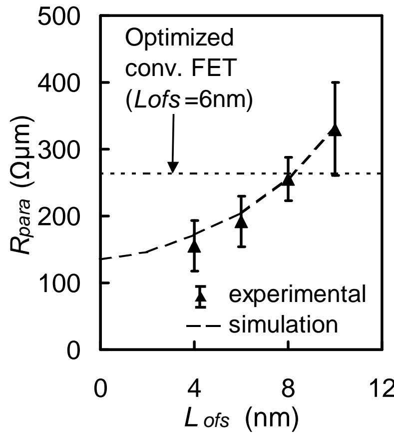


Fig. 7 Saturation R_{para} of DSS FET as a function of L_{ofs}. A broken curve shows simulated results. A horizontal dotted line indicates R_{para} of optimized conv. FET.

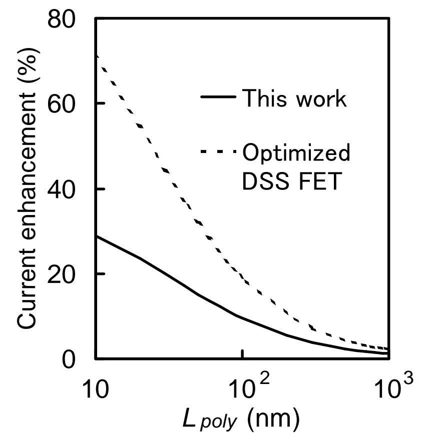


Fig. 8 Drive current enhancement of DSS over conv. FET, which is defined by $R_{para}^{conv}/R_{para}^{DSS}$ at sufficiently high V_{ov}.