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Carbon Nanotube Via Technologies for Advanced Interconnect Integration

Mizuhisa Nihei[1,2], Akio Kawabata[1,2], Takashi Hyakushima[1], Shintaro Sato[1,2], Tatsuhiro Nozue[1], Daiyu Kondo[1,2], Hiroki Shioya[1,2], Taisuke Iwai[2,3], Mari Ohfuti[1,2] and Yuji Awano[1,2]
[1] MIRAI-Selete (Semiconductor Leading Edge Technologies, Inc.)
[2] Fujitsu Limited
[3] Nanotechnology Research Center, Fujitsu Laboratories Ltd.,
10-1, Morinosato-wakamiya, Atsugi, Kanagawa 243-0197, Japan
Phone: +81-46-248-3280, Email: nihei.mizuhisa@selete.co.jp

Abstract

We developed planar carbon nanotube (CNT) vias and their low-temperature fabrication processes consisting of low-temperature CNT growth and chemical mechanical polishing (CMP) of the CNT bundles. We were able to lower the CNT growth temperature to 400°C, which meets the requirement to avoid thermal damage to LSIs. Not only was the CMP effective for planarization; it also lowered the via resistance by about 25% with improved distribution. Our low-temperature planar CNT via technologies are very promising for the achievement of low-resistance scaled-down CNT vias for future LSI interconnects.

1. Introduction

CNTs exhibit excellent electrical properties that include current densities exceeding 10^9 A/cm^2 [1] and ballistic transport up to several micrometers along the tube [2]. Because of these factors, with their large electro-migration tolerance and low electrical resistance CNTs can be used as nano-size wiring materials, and are thus becoming potential candidates for future LSI interconnects. Much effort has been made to produce CNT vias [3-5], which use bundles of metallic MWNTs (multi-walled carbon nanotubes), as vertical wiring materials as shown in Figure 1. Sato *et al.* demonstrated low-resistance CNT vias employing a novel metallization technology, which used preformed catalyst metal particles, to grow dense MWNTs by thermal chemical vapor deposition (CVD) [5]. The resultant CNT-via resistance was of the same order of magnitude as that of W plugs, which is the lowest ever reported. However, no special planarization processes have been taken into consideration, and these are actually required for LSI interconnect integration. Instead, Horibe *et al.* developed planar CNT vias that are polished mechanically with diamond slurry [6]. In order to integrate CNT vias with the next generation of low-k materials, CMP planarization − which basically uses a chemical process − is required to avoid damaging these materials with their low mechanical strength. Similarly, low-temperature fabrication processes below 400ºC are also needed for LSI interconnect integration, because the low-k materials and MOSFETs in LSIs have a low thermal tolerance.

In this paper, we describe low-temperature CVD growth of well-graphitized high-quality MWNTs at as low as 400ºC using preformed Co catalyst particles on a TiN contact layer. We also describe planar CNT via fabrication processes using CMP and a room-temperature top metal contact process, resulting in lower electrical resistance with better uniformity than in non-planar CNT vias.

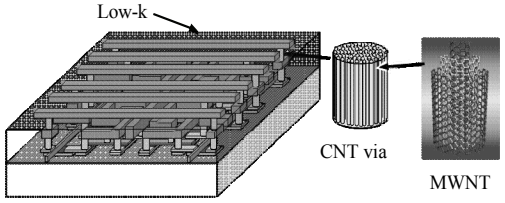

Fig 1. Schematic of future LSI interconnects consisting of CNT vias and low-k materials.

2. Experimental

Figure 2 is a schematic of the process we used to integrate a CNT via and Cu wire. The fabricated substrate was composed of Cu wiring (100 nm thick), a Ta barrier layer (15 nm), a TiN contact layer (5 nm), and a tetraethylorthosilicate (TEOS) dielectric layer (270 nm). Via holes were made using conventional photolithography and subsequent wet etching with a buffered HF solution. Size-controlled Co particles with an average diameter of about 4 nm were then deposited on the substrate using a catalyst nano-particles deposition system [5]. For CNT growth using the thermal CVD system, a mixture of C_2H_2 and Ar at 1 kPa was used as the source gas. The substrate temperatures used in this study were 400ºC and 510ºC. The CMP process we used is as follows: the spin-on glass (SOG) was coated on the samples in order to hold the CNT bundles during the CMP process. The sample was polished with a conventional IC1000 pad and silica slurry under pressures of 2 psi (13.8 kPa) for 150 sec. Finally, the Ti top contact layer (50 nm) and Cu wire (300 nm) were connected to CNT vias by metal deposition without subsequent annealing.

3. Results and Discussion

Figure 3(a) shows a SEM image of CNT vias formed by thermal CVD at a growth temperature of 400ºC. We have succeeded in growing vertically-aligned CNT bundles in 2-μm diameter via holes. Figure 3(b) shows a TEM image of an MWNT formed at 400ºC. We were able to obtain about six walled MWNTs with an outer diameter of about 7 nm, having a higher quality of graphite sheets than in our previous studies, even at 400ºC. The improvement in the CNT's quality is due to the optimization of the growth conditions by diluting the C_2H_2 source gas with Ar carrier gas.

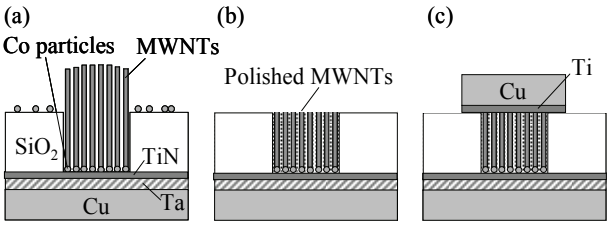

Fig. 2. CNT via process: (a) Fabrication of via hole structure, deposition of Co particles and MWNT growth; (b) CMP planarization of MWNTs; (c) Fabrication of top metal contact.

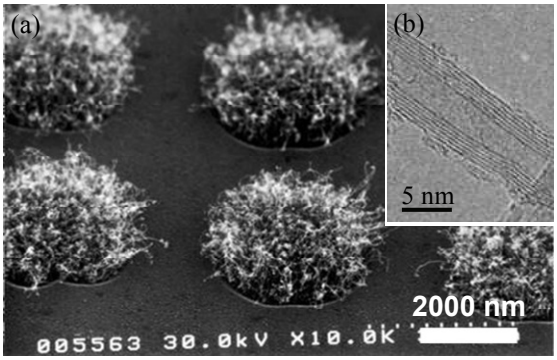

Fig. 3. (a) SEM images of bundles of MWNTs in 2-μm-diameter vias and (b) TEM images of a MWNT grown by thermal CVD at 400ºC using Co nano-particle catalysts.

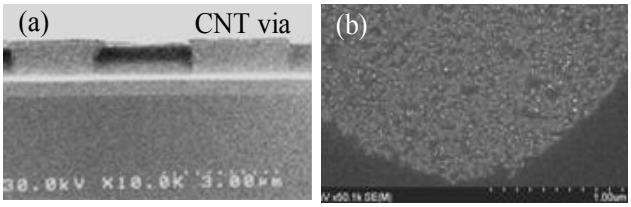

Fig. 4. (a) Cross-sectional and (b) in-plane SEM images of CNT vias after CMP planarization

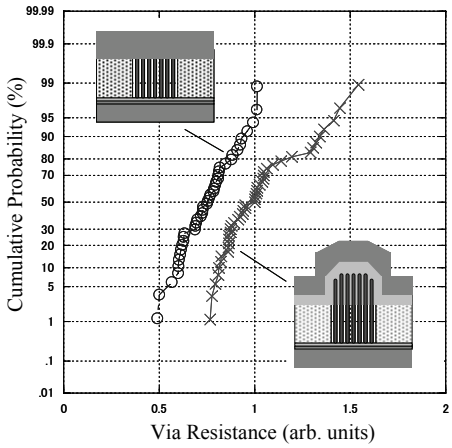

Fig. 5. Via resistance depending on the top metal contacts with and without CMP planarization.

Figures 4(a) and (b) show cross-sectional and in-plane SEM images of CNT vias after CMP planarization, respectively. The CNT growth temperature of this sample is 510°C. The top portion of the CNT bundles was successfully polished under pressures as low as in the conventional Cu/low-k CMP process. The circular structures of an MWNT's tip were clearly observed in the 2-μm-diameter via area. We were able to obtain ohmic contact between these MWNT tips and the top metal electrode without annealing, which is also a favorable low-temperature fabrication process.

We measured the via resistance with a four-point probe at room temperature using Kelvin patterns. Figure 5 shows via resistance distributions of the 2-μm-diameter CNT vias with and without CMP planarization. The average via resistance of the sample with CMP decreased by about 25% compared with that without CMP. The scattering for the distribution of the sample with CMP is also smaller than that without CMP. We speculated that cutting the CNT bundles short by CMP could increase the number of electrical contacts between MWNT tips and the top metal electrode, because as-grown CNT bundles have an unfavorable worse uniformity in length.

4. Conclusions

We developed planar CNT vias and their low-temperature fabrication processes which meet the requirement to avoid thermal damage to LSIs. We achieved low-temperature CVD growth of MWNTs at as low as 400ºC. Our planar CNT vias, fabricated using a CMP under pressures as low as conventional Cu/low-k CMP, resulted in electrical resistances improved by about 25% and a small scattering in distribution.

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