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Ti-barrier Metal for Robust and Reliable 45nm Node Porous Low-k/Copper Interconnects

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Abstract

We demonstrate the excellent properties of titanium (Ti) as a barrier metal (BM) for 45nm node porous low-k/Cu interconnects. Wider margin for Q-Time between seed-Cu deposition and Cu electrochemical plating (ECP) was verified in Ti-barrier process. Excellent reliability, such as time dependent dielectric breakdown (TDDB), electromigration (EM) and stress-migration (SM) endurance, was confirmed by using Ti-barrier. Moreover, the constraint of dummy pattern design for suppressing moisture induced via failure (MIVF) can be drastically relaxed by higher oxidation resistance of Ti-barrier.

Introduction

In porous low-k/Cu integration for 45nm node high performance devices, MIVF has been reported to be one of the serious issues.[1],[2] The porous low-k film is easily damaged during plasma processes and absorbs moisture in damaged layer. The moisture oxidizes barrier material and causes stress-induced voiding (SIV) failure.[3],[4] Thus, developing oxidation resistant BM process is one of the most important approaches for robust and reliable porous low-k/Cu integration. In this paper, we demonstrate the advantage of Ti as a superior barrier material for Cu in terms of reliability and from the viewpoint of dummy design.

Experimental

Stacked SiOC(k=2.3)/PAr(k=2.3) structure (Hybrid) with 45nm-node design was used in this experiment. Because the wettability of Cu on Ti is superior to that on Ta[5], we investigated the via chain yield by controlling the Q-Time between seed-Cu deposition and Cu ECP from ASAP to 7days. We carried out TDDB test (Tc=325 ºC, E=1.5MV/cm), SM (Tc=175ºC for 1000hours) and EM test (Tc=325/340ºC, J=6 MA/cm^2), in order to evaluate the process impact on the reliabilities. Moreover, we evaluated the resistance of via Kelvin module surrounded by variety of dummy pattern to clarify the relations between via resistance increase caused by BM oxidation and dummy pattern layout. 25% higher degassing temperature before BM deposition was experimentally performed to identify the influence of moisture inside low-k film on resistance increase.

Results and Discussion

A. Effect of Ti-barrier

Q-Time, between seed-Cu deposition and ECP, dependence on via chain yield is shown in Fig.1. In both BM cases, yield degraded with longer Q-Time. But Ta-barrier showed faster yield degradation than Ti-barrier process, and this result indicates the better stability of Cu on Ti-barrier.

B. Evaluation of reliability

Figure 2 shows the TDDB result, comparing Ta-barrier process with Ti-barrier process. Even in the case of the thin film thickness of 5nm, no degradation was observed by using Ti-barrier. EM reliability test result is shown in Fig.3. Improvement of EM lifetime of 1.5~2 orders was realized in Ti-barrier process. It is considered that good adhesion between Ti and Cu and/or diffused Ti into Cu grain boundaries suppressed Cu migration.[6] Figure 4 shows the comparison data of SM endurance with Ta-barrier and Ti-barrier. No failure was observed in the “with dummy” case, but M2-wide pattern without dummy failed in Ta-barrier process. Moisture in porous low-k film oxidized the BM, causing the SIV failure by poor adhesion between oxidized BM and Cu. The fact that no SIV failure was observed in Ti-barrier process indicates higher oxidative resistance of Ti barrier.

C. Impact of Ti-barrier on the dummy pattern layout

Figure 5 shows the outline of test pattern designed to evaluate the influence of dummy pattern on via resistance. The measurement pattern consists of two vias connected with island-like upper wiring surrounded with the various dummy patterns. Figure 6(a) shows distances from via to dummy pattern dependence on resistance increase by using pattern A. The via resistance increased if the dummy pattern was placed not less than 3um from the via, indicating that the area where removable moisture exists is within 3um from a via. Moreover, the area is changed little by increasing degassing temperature. Figure 6(b) shows area size dependency on via resistance increase by using pattern B. The via resistance increased as the dummy area shrank, and it was found that the moisture which exists in hundreds of micron area affected the resistance. Figure 6(c) shows dummy pattern density dependence on resistance increase by using pattern C. Resistance increased as dummy density became lower, and the resistance increase rate was suppressed by adoption of higher degassing temperature and Ti-barrier. Figure 7 shows the dependence of via resistance

on local and global dummy density by using pattern D. The resistance increased as local/global dummy density became lower. The required dummy density for suppressing resistance increase by oxidation of BM could be drastically relaxed by utilizing Ti as a barrier material.

Conclusions

A robust and reliable porous low-k/Cu integration was developed by utilizing Ti as a barrier material for Cu. Reliability improvement, such as SM and EM, was realized due to the good adhesion of Ti to Cu. The influence of oxidation of BM by moisture absorbed in porous low-k ILD was suppressed by using Ti-barrier because of its higher resistance to oxidation.

Acknowledgements

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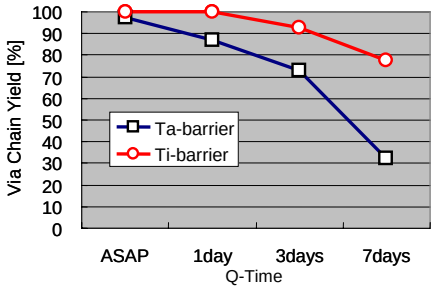

Fig.1 Via chain yield dependence on Q-Time between Seed-Cu deposition and Cu ECP.

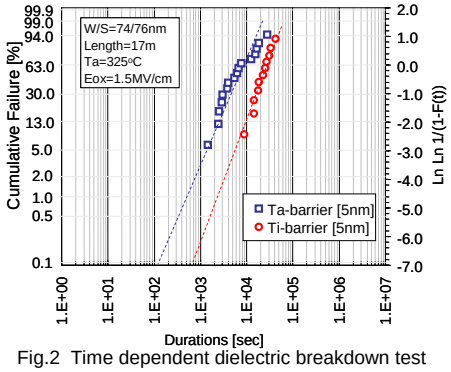

Fig.2 Time dependent dielectric breakdown test (TDDB) results

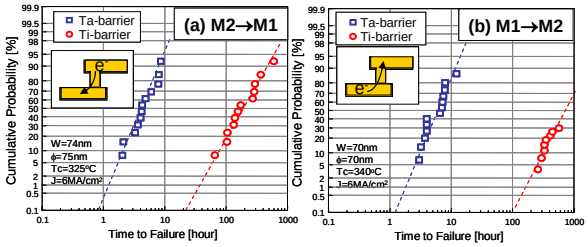

Fig.3 Electromigration test results. The e-flow is (a) from M2 to M1, (b) from M1 to M2.

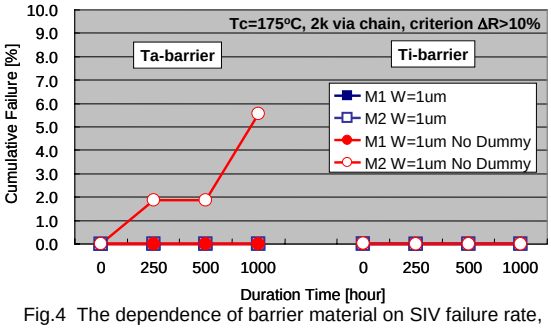

Fig.4 The dependence of barrier material on SIV failure rate, with and without metal dummy pattern surrounding the test pattern.

Pattern	Varied Parameter
A	Distance from via to dummy pattern(0.14um~10um)
B	Dummy Pattern Area Size(6um~400um)
C	Dummy Pattern Density (0.2%~64%)
D	Local/Global Dummy Density (Ld/Gd=0.2~34.4/0~5.9%)

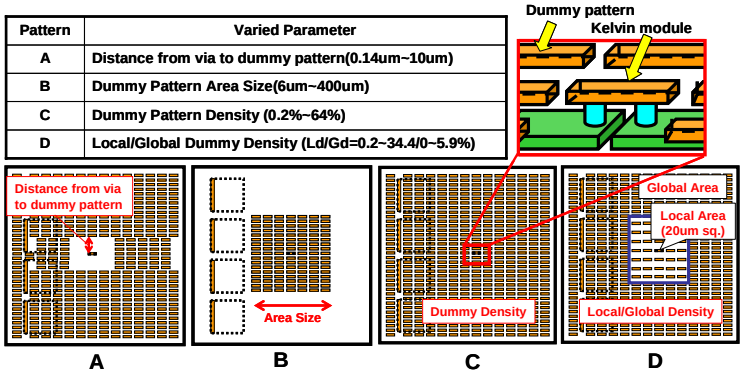

Fig.5 Test pattern structures to evaluate the barrier metal oxidation by moisture coming from porous low-k ILDs.

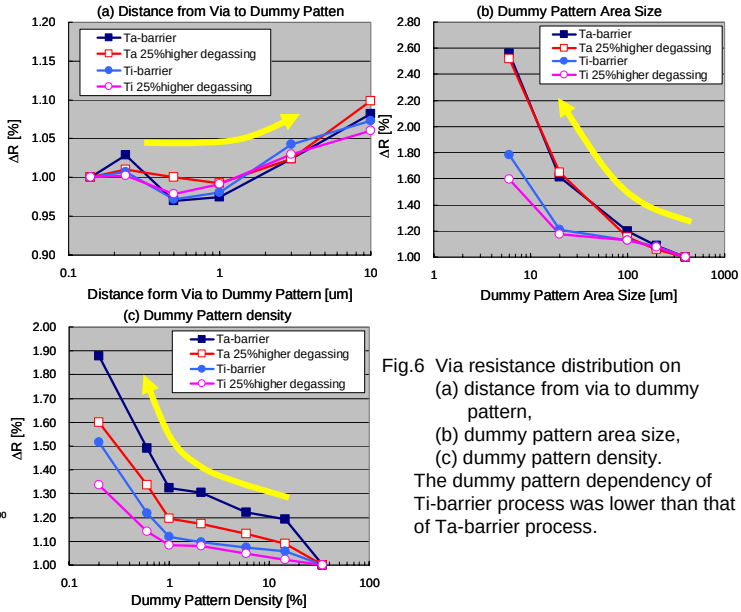

Fig.6 Via resistance distribution on
(a) distance from via to dummy pattern,
(b) dummy pattern area size,
(c) dummy pattern density.
The dummy pattern dependency of Ti-barrier process was lower than that of Ta-barrier process.

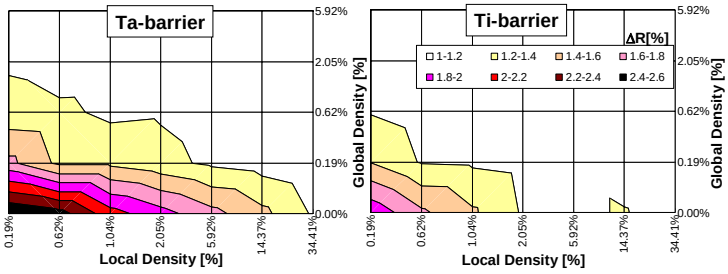

Fig.7 Dependence of via resistance on local dummy density and global dummy density. The required density necessary for suppressing resistance increase is relaxed by using Ti-barrier.