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Key mechanisms for improved EM lifetime of CoWP capped Cu interconnects

Yumi Kakuhara¹, Naoyoshi Kawahara¹, Kazuyoshi Ueno² and Noriaki Oda^{1*}

¹NEC Electronics Corporation, Advanced Device Development Division 1120 Shimokuzawa, Sagamihara, Kanagawa, 229-1198 Japan

Phone: +81-42-771-0707 E-mail: yumi.kakuhara@necel.com

²Shibaura Institute of Technology, Dept. of Electronic Engineering

3-7-5 Toyosu, Koto-ku, Tokyo, 135-8548 Japan

1. Introduction

CoWP capped Cu interconnects have been evaluated for its high Electromigration (EM) reliability. Cu/cap interface diffusion is suppressed by strong adhesion between CoWP and Cu [1]. In addition, Co diffusion in Cu affects the long EM lifetime and the high activation energy [2]. To know what factor is more important to achieve the best performance for reliability is necessary for applying this technology. Especially, the effect of Co diffusion is unknown for the low temperature (under 350°C). In this study, the dependence of EM failure for CoWP capped Cu interconnects on the EM test temperature was investigated.

2. Experiment

Fig. 1 (a) shows the schematic cross-section of two level Cu single damascene interconnect used in this study. CoWP was deposited on the M1 Cu lines only. As an interlayer dielectrics, SiO₂ was used for the M1 level and SiOC was used for the via and the M2 levels. SiCN was deposited on the CoWP capped M1 lines with or without NH₃ plasma pre-treatment. Fig. 1 (b) shows the EM test structure used in this study [3][4]. There are the five M1 level interconnects terminated with the vias connected to the M2 level interconnect in parallel and the 4 units are connected in series. The 20 via-line segments are tested with one sample. The M1 width and the M1 length are 0.12µm and 100µm, respectively. The via diameter is 0.14µm. The EM tests were performed at the current density of 2MA/cm² and at the test temperatures of 275, 300, 350 and 380 °C. The failure criterion was defined as the time at which the first (weakest) via failed, then EM lifetimes were plotted with the failure distribution per a via-line segment [3] [4]. In this experiment, the 200 line-via segments (20 via-line segments x 10 samples) were measured for the EM life time plot, so the lower failure probability can be measured which is more important to the critical failure estimation $(ex. t_{0.1}).$



Figure 1. Schematic illustration of (a) the cross-section of the EM test sample. (b) plan-view of test structure

*Now he is with Semiconductor Leading Edge Technologies, Inc.

3. Result and discussion

EM life time for different test temperature

Fig. 2 shows the EM lifetime plots for the different test temperatures. The dispersion of EM lifetime became wide as the test temperature rose, because the dependence of EM lifetime on the test temperature became weak (w/ p-NH₃) or disappeared (w/o p-NH₃) for higher failure probability. The EM lifetime and σ were plotted as the function of the inversion of the test temperature in Fig. 3. Ea is obtained from a slop of plots usually, but it is not appropriate to apply that method to these plots because σ changed widely for the different temperatures. This indicates the existence of the multi-EM mechanism mode. During the EM tests, the resistance increased slightly regardless w/ or w/o NH₃-plasma treatment due to Co diffusion in Cu [2]. We thought that the high temperature storage during the EM test accelerated Co diffusion in Cu, so the EM failure was suppressed as the test temperature rose.







Figure 3 (a) EM life time (t3.3), (b) σ vs.1/T. Estimation of Ea is inappropriate due to wide change of σ (indicating multi-EM mode).

EM failure analysis

In Fig. 4 (a), EM failure void was observed in the line away from the via, not under the via as it is observed for the Cu interconnects commonly. Similar void generation was observed for other EM failed samples. CoWP remained under the via (Fig.4 (b)) after the via etching. The existence of CoWP was thought to suppress the void generation under the via where the microstructural damage existed due to the via hole formation. The long EM lifetime for CoWP capped Cu lines must be attributed to the void formation in the lines as the void volume was larger than its under the via in case of the conventional Cu lines. In Fig. 4(c), a weak contrast point at the top of the EM void indicated that the CoWP deposition was incompletely. It was speculated that this part became a void nucleation site.



Figure 4. (a) TEM image of the EM void (b) CoWP remains under via (c) Incomplete CoWP deposition at EM void

Mechanism of EM failure at high test temperature

The mechanism of EM failure was thought to be affected by the test temperature for the evaluated CoWP capped Cu interconnects. In Fig. 5, TEM cross section for the CoWP capped Cu line shows that the CoWP deposition was incomplete in the vicinity of the barrier metal. The EM void nucleation site could be the more incomplete CoWP deposition point. EDX analysis showed Co diffused in the vicinity of the Cu/barrier metal interface, not in the bulk Cu. It was speculated that Co diffused in Cu with the high EM test temperature and reinforced the void nucleation site where the CoWP deposited incompletely (Fig.6). This effect was encouraged as the temperature rose, so EM failure was suppressed and EM lifetime became long at the higher temperature. Considering the effect of NH₃-plasma treatment, it is speculated that the NH₃-plasma treatment made the reinforcement weak a little due to the Cu nitride [5] for the incomplete CoWP deposition point.



Figure 5. TEM image of Cu line cross-section . EDX observation for Point A showed Co diffusion in Cu in the vicinity of barrier metal , Co was not detected for Point B.





Figure 6. Model for effect of Co diffusion. The potential void nucleation site was reinforced with Co diffusion.

4. Conclusion

Evaluating the CoWP capped Cu interconnects, EM lifetime tended to become longer as the test temperature rose .The cause of this phenomenon was estimated that Co diffusion in the Cu/barrier metal interface was accelerated by the rising test temperature then strengthened the vulnerable void nucleation sites due to the incomplete CoWP deposition. It is impossible to come into effect of the Co diffusion with the wafer processing temperature. So capping the Cu interconnects (including under vias) with CoWP completely is the most essential factor to achieve the highest reliability performance because it can eliminate the void nucleation site, then make the most of the excellent Cu/CoWP interface property.

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