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A MOCVD TiSiN/Ta Barrier Metal for Improved EM Performance and Low Via/line Resistance using Direct Contact Via (DCV) Process for Sub-65 nm Technology

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Abstract

Integration of MOCVD TiSiN barrier metal with low-k dielectric layer (k=2.9) has been successfully demonstrated for 65 nm technology. By eliminating TiSiN barrier at via bottom prior to Cu via formation using Direct Contact Via (DCV) process, electromigration (EM) reliability of the TiSiN barrier was found to be substantially improved. Also, a significant reduction of 0.1 um via/line resistances is achieved. The proposed integration method allows MOCVD TiSiN barrier usable for nano interconnect, being able to take advantage of high throughput and excellent step coverage of MOCVD process.

Introduction

Tantalum-based PVD barriers used in advanced CMOS technology may begin to show marginality and lead to device failures as interconnect feature sizes continue to scale down below 0.1um[1]. Recently, atomic layer deposition (ALD) was proposed as the barrier deposition method due to its excellent coverage ability, but some issues, such as low throughput and poor reliability, need to be resolved for manufacturing[2,3]. As an alternative barrier material, MOCVD TiSiN was investigated because it can provide good coverage with high throughput and ability of suppressing Cu diffusion[4]. However, a satisfactory EM performance has yet been reported [4]. The purpose of this work is to investigate the feasibility of MOCVD TiSiN barrier metal assisted with Direct Contact Via (DCV) process for EM improvement and 65 nm low-k backend process.

Fabrication

A TiSiN film was prepared by the reaction with SiH_4 gas on a TiN layer formed through H_2+N_2 plasma using TDMAT precursor. The TiSiN layer was deposited at 350℃ on the dual damascene structure made of a SiOC low-k dielectric (k=2.9). DCV process was performed using DC-biased Ar+ plasma to remove the TiSiN layer at via bottom in a PVD Ta chamber (Fig.1). A Ta deposition was followed in-situ after the selective removal of the TiSiN.

Results and Discussion

In order to confirm copper diffusion barrier property of a single layer of TiSiN, Cu concentration within the low-k dielectric was measured using Vapor Phase Decomposition (VPD) analysis after 1 hr anneal at 350℃ (Table 1). The diffusion barrier property of TiSiN and TiSiN/Ta was found to be very similar to one of TaN/Ta. Also we analyzed diffusion behavior of Cu into the TiSiN barrier under various anneal conditions by AES (Fig.2). According to the AES result, the TiSiN barrier showed good barrier stability regardless of the anneal temperature. However, the PVD TaN/Ta barrier showed unstable behavior after 1 hr anneal at 600℃. Based on the results, the TiSiN film appears to have better diffusion barrier property than that of the TaN/Ta. For adhesion strength evaluation, a tape test was done. Adhesion property of TiSiN with the oxide dielectric and the seed Cu was found to be as good as that of PVD TaN/Ta. Fig. 3 shows SEM images of Cu deposited on the different barrier metals for checking adhesion. Note that Cu agglomerates on the single TaN layer after 350℃ anneal in Fig. 3a but the morphology for the other barriers has no Cu agglomeration. The change in the morphology correlates with the reflectivity change shown in Table 2. It is found that adhesion property of single TiSiN film is similar to conventional PVD TaN/Ta barrier metal. Good coverage of TiSiN in the damascene structure was confirmed by TEM and EELS analysis (Fig.4 and Fig.5). Compared to non DCV process (Fig.4), successful removal of TiSiN at the bottom of the via is clearly seen in the DCV process (Fig.5). Electrical properties of the DCV TiSiN/Ta are compared against TaN/Ta and TiSiN barrier. The via resistance (Rc) and metal resistance (Rs) were measured for varying barrier metals deposited on the dual damascene structure (Fig.6). The Rc reduced as the thickness of the TiSiN decreased (Fig.6). Despite the higher Rc value of TiSiN/Ta bilayer than that of TaN/Ta bilayer, the Rc of the TiSiN/Ta prepared using the DCV process was found to be dramatically reduced. It clearly indicates that the DCV process helps to lower the via resistance as well as the line resistance in both TiSiN/Ta and TaN/Ta barriers. In addition, the Rs of TiSiN prepared using the DCV is lower than that of PVD TaN/Ta, which is believed to be due to the thin TiSiN thickness at the bottom of a line trench, as shown in Fig. 7. Fig. 8 shows the reliability performance of the barriers tested by Vramp leakage current test up to 5 MV/cm at 125℃. Fig. 9 shows the varying barrier metals have a similar tendency in the leakage current as the temperature increases from 20 °C to 125 °C. The effect of the DCV process on the leakage current between two adjacent lines looks insignificant. EM test was performed under the condition of 2 MV/cm at 350℃. Table 3 and Fig. 10 show that the DCV TiSiN/Ta has a comparable EM performance to conventional PVD TaN/Ta. Note that EM performance of a single TiSiN barrier was very poor compared to the DCV TiSiN/Ta. The poor EM performance of the single TiSiN film can be recovered by performing the DCV process and the subsequent Ta deposition. The enhanced EM lifetime is believed to result from both the reduced via resistance obtained using the DCV process and the increased volume fraction in the Cu(111) plane, led by β-Ta(002) formation [5]. We also think that EM life time is influenced by the enhancement of adhesion property between TiSiN and seed Cu by thin Ta.

Conclusion

We report highly improved EM performance and via/line metal sheet resistance of 65 nm interconnects composed of MOCVD TiSiN/Ta barrier metal by integrating DCV process in the low-k backend process. The DCV process enables to selectively remove TiSiN at the via and the trench bottoms, leading to a significant reduction of the via/line resistance and the improvement of the EM performance. The presented technique allows the MOCVD TiSiN usable as the barrier metal for 65 nm technology and can be readily applicable to next node technology thanks to the excellent step coverage of the MOCVD process at the nanoscale contacts/vias.

References

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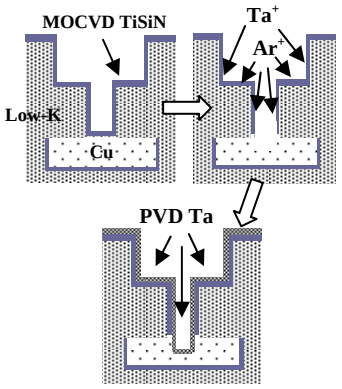

Fig.1 Schematic illuminations of DCV TiSiN/Ta deposition process.

Film structure	Cu conc. (atom/cm^2)
low-k 300 nm/TaN 15 nm /Ta 15nm/seed Cu/ECP Cu	6.78 E + 10
low-k 300 nm/TiSiN 5nm/ seed Cu/ECP Cu	8.11 E + 10
low-k 300 nm/TiSiN 5nm/Ta 3nm/ seed Cu/ECP Cu	4.06 E + 10

Table 1 VPD Analysis results of Cu concentration within low-k film after CMP and DHF cleaning.

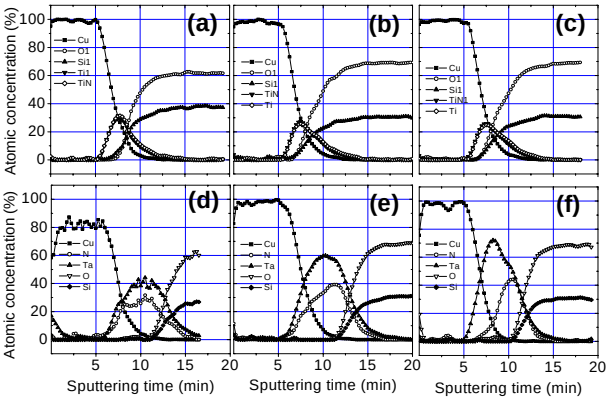

Fig.2 AES analysis results of TiSiN/Cu and TaN/Ta/Cu as a function of temperature (a) TiSiN, 600℃, (b) TiSiN, 500℃, (c) TiSiN, 400℃, (d) TaN/Ta, 600℃, (e) TaN/Ta, 500℃, (f) TaN/Ta, 400℃

film	R_{ini}(%)	R (%)	R/R_{ini}
TaN/Ta	124	119	95.9
TiSiN	121	117	96.6
TiSiN/Ta	124	112	90.3
TaN	120	78	65

Table 2 Reflectivity changes of Cu film deposited on different barrier metals after anneal. R_{ini} and R indicate reflectance prior to anneal and after 1 hour anneal at 350℃, respectively.

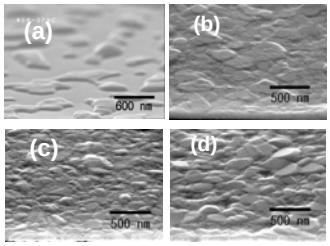

Fig.3 SEM image of Cu surface after 1 hour anneal at 350℃ on different types of barrier metal. (a) TaN/Seed Cu, (b) TaN/Ta/Seed Cu, (c) TiSiN/Seed Cu, (d) TiSiN/Ta/Seed Cu.

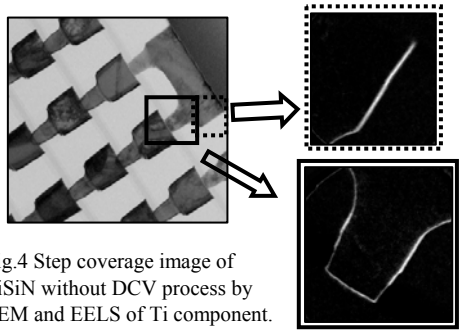

Fig.4 Step coverage image of TiSiN without DCV process by TEM and EELS of Ti component.

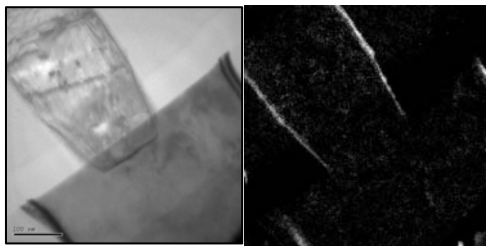

Fig.5 Step coverage image of TiSiN/Ta with DCV process by TEM and EELS of Ti component.

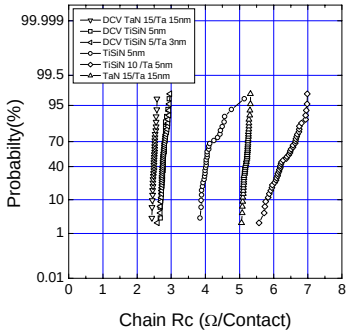

Fig.6 Via resistance of 0.10 um chain pattern as a function of TiSiN and TaN/Ta structure.

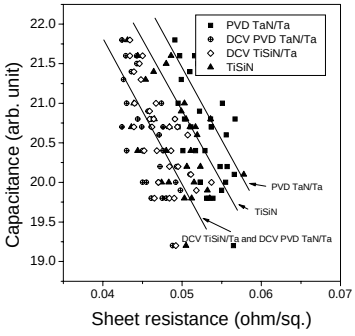

Fig.7 Capacitance vs. sheet resistance of Cu/ low-k with various barrier processes.

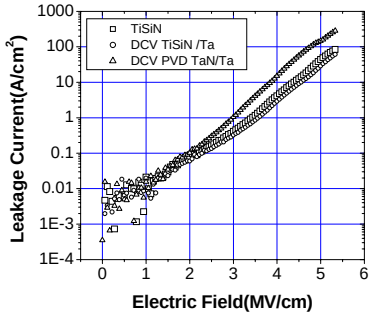

Fig.8 Effect of barrier metal on leakage current at 125℃ as a function of electric field

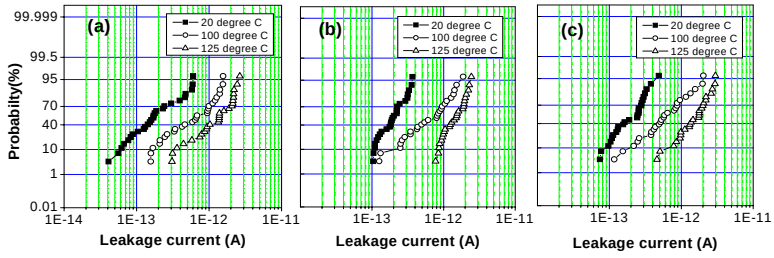

Fig.9 Leakage current in dual damascene pattern as a function of temperature. (a) TiSiN (b) DCV TiSiN/Ta (c) DCV PVD TaN /Ta .

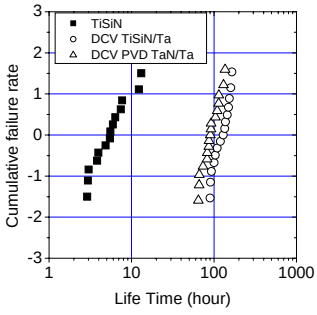

Fig.10 EM lifetime of TiSiN, DCV TiSiN/Ta and DCV PVD TaN/Ta measured under 2MV/cm at 350℃.

Item	Barrier metal structure		
	TiSiN	DCV TiSiN/Ta	DCV PVD TaN/Ta
MTTF (hour)	5.45	113.5	91.7
σ	0.57	0.28	0.26
Life time (year)	3	172	144

Table 3 MTTF and EM lifetime results of TiSiN, DCV TiSiN/Ta and DCV PVD TaN/Ta under 2MV/cm at 350℃.