Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 148-149

G-1-5

Modeling and Characterization of the On-chip Interconnects

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1. Introduction

It is well know that interconnect delay has become more significant vis-à-vis the gate-delay with the aggressive scaling of the feature size in CMOS technology. Further, with ever increasing circuit speeds, effect of the inductance due to interconnect on the signal propagation has become too important to be ignored. The on-chip interconnects are modeled using different equivalent circuits in literature. In this paper, we present extraction of different models for on-chip interconnects with width ranging from 100 nm to 2 µm and length ranging from 500 µm to 2 mm. Multiple sections of the models are used for accurate representation of different lengths of the interconnect and SPICE simulations are used to simulate the delay. The effect of the interconnect-inductance and resistance are clearly identified with these simulations thus indicating the application of RF models in time domain characterizations.

2. Test structures and model extraction

Copper interconnect lines of widths ranging from 100 nm to 2 µm and lengths ranging from 500 to 2000 µm were fabricated on a Si substrate with a deposited oxide of ~10 µm thickness. Thicker isolation oxide is in the range of the total dielectric thickness achieved in standard 8-10 metal level processes. The interconnect-lines were designed in Ground-Signal-Ground configuration (Co-planar waveguide (CPW) configuration with widely separated ground bars to suppress the excitation of CPW modes) for RF characterization. The process details are available elsewhere [1]. S-parameters were measured from 50 MHz to 40 GHz using HP8510C network analyzer. Line-reflect-reflect-match (LRRM) techniques were used to calibrate the network analyzer. The interconnect lines were modeled as multiple cascaded sections of a standard transmission line based on telegrapher's equations (Telegrapher's model, Fig. 1(a)) as well as a wide-band model [2]. Wide-band model (Fig. 1(b)) takes into account the effect of substrate and the skin effect. These models were extracted using IC-CAP modeling tools [3]. The model parameters were calculated using asymptotic techniques described in [2]. The models were further refined using non-linear optimization routines available in IC-CAP. Typically, the magnitude and phase r.m.s. errors were below 3.8 percent. These models were used for time domain simulation using pulses with different rise/fall times at the input.

3. Results and discussion

Fig. 2 shows magnitude and phase of the s-parameters modeled using telegrapher's model [Fig. 2(a)] and wide-band model [Fig. 2(b)] for a 2 µm wide and 500 µm long interconnect line. It is discernible that the wide-band model represents the s-parameters more accurately over the entire frequency range. The same trend was observed for all interconnect lines with width ranging from 100 nm to 2 µm and lengths ranging from 500 µm to 2000 µm. It may be mentioned here that 3, 6 and 12 cascaded sections were used for 500, 1000 and 2000 µm long lines respectively. The r.m.s. errors between measured and simulated s-parameters for 12 sections 2000 µm long lines were below 3.3 and 1.7 percent for telegrapher and wide-band models respectively. Overall wide-band model showed better fit between measured and experimental s-parameters data as compared to telegrapher's model. The optimized model parameter values were taken as frequency independent. Input pulses with rise/fall time varying from 10 to 50 ps were used in SPICE simulations.

Fig. 3 shows the output pulse of line widths 100, 250 and 2000 nm simulated using both telegrapher and wide-band models. The inductive effect is more evident for wide-band model as compared to Telegrapher's model resulting in relatively faster rise/fall time for smaller line widths of 100 nm. For larger line widths of 250 and 2000 nm the amplitude of overshoots and undershoots is more for wide-band model indicating enhanced inductance effect with wide-band model

Fig.4 shows that the attenuation of the pulse amplitude increases with increase in length due to increased resistance of the interconnect lines. Therefore rise/fall time for smaller line-widths of 100 and 250 nm increases with length. The ringing amplitude for larger line width of 2000 nm decreases with length due to increase in line resistance masking the effect of inductance.

Fig.5 shows the input/output pulse shapes for rise and fall time of 10, 25 and 50 ps for a line width of 100 nm. A 100 nm wide line will have higher resistance as compared to 2000 nm wide line. A pulse with smaller input rise/fall time will have more high frequency components than a slowly rising pulse. We have also observed that the attenuation constant alpha of the interconnect lines is frequency dependent and increases with the increase in frequency. Therefore output of a pulse with a shorter input rise/fall time is attenuated more as compared to a pulse with a longer rise/fall time due to relatively higher attenuation of high frequency components [4]. Thus an output pulse with larger rise/fall time resembles closely to an input pulse due to less attenuation as is evident in Fig. 5.

Fig. 6 shows the effect of change of rise/fall time on an interconnect line of 2000 nm width. The wider interconnect line have less resistance and larger inductive effect resulting in ringing of the output signal than the interconnect line of smaller width of 100 nm due to decrease in its resistance. The effect of larger input rise/fall time is decrease in overshoot/undershoot amplitude indicating that these lines can be represented by RC models.

4. Conclusion

Multi-section wide-band models have been extracted and used for simulating the delay. It is observed that the wider interconnects, the inductance has significant impact on the delay while for narrower interconnects, the series resistance masks the inductive effect. Multiple sections of telegrapher and wide-band model have helped in improving the wide-band representation of interconnect lines. Wider and longer interconnect lines are more accurately represented by wide-band model. Further, the application of the models extracted using RF techniques is shown for the time domain analysis.

References

[1] R. Kumar et al., Proc. 22nd AMC, 33-36 (2006)
[2] S. Sun et al., IEEE RFIC Conf. 2006
[3] IC-CAP User's guide, Agilent Technologies (2002)
[4] Y.I. Ismail, IEEE Trans. On VLSI, vol. 10, no. 6, 685-694 (2002)

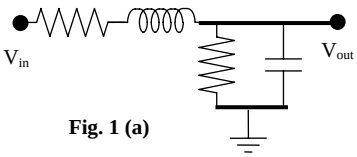

Fig. 1 (a)

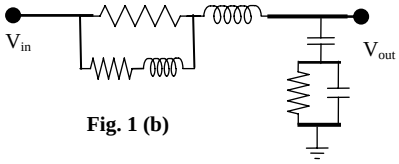

Fig. 1 (b)

Fig. 1 Single section circuit schematic of (a) Telegrapher model and (b) Wide-band model

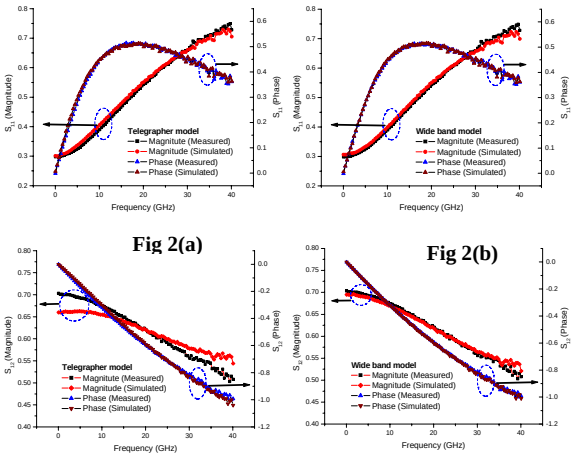

Fig 2(a)

Fig 2(b)

Fig 2(c)

Fig 2(d)

Fig. 2 Magnitude and phase of measured and simulated S-parameters for a line of W=2 µm and L=500 µm, (a) S_{11} , telegrapher model, (b) S_{11} Wide-band model, (c) S_{12} , telegrapher model, and (d) S_{12} Wide-band model

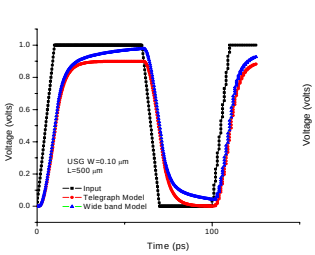

Fig 3(a)

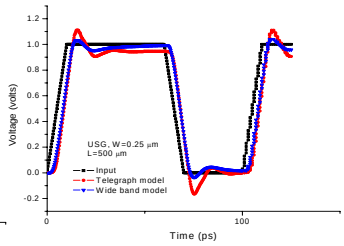

Fig 3(b)

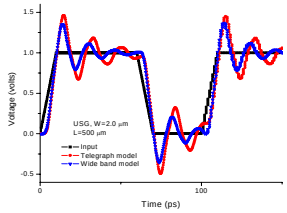

Fig 3(c)

Fig. 3 Input and output pulse shapes (telegrapher and wide-band models) for a line length of 500 µm and line widths of (a) 100 nm, (b) 250 nm, and (c) 2000 nm

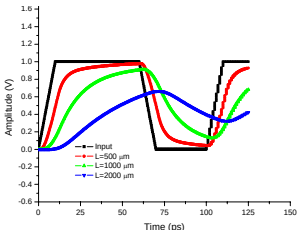

Fig 4(a)

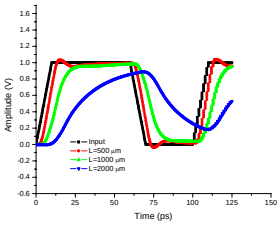

Fig 4(b)

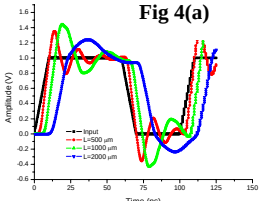

Fig 4(c)

Fig. 4 Input and output pulse shapes (wide-band model) for line lengths of 500, 1000 and 2000 µm and line widths of (a) 100 nm, (b) 250 nm, and (c) 2000 nm

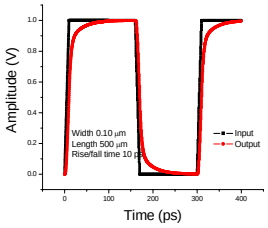

Fig 5(a)

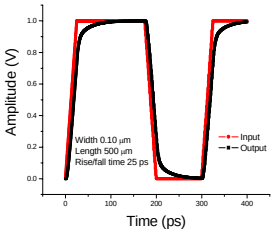

Fig 5(b)

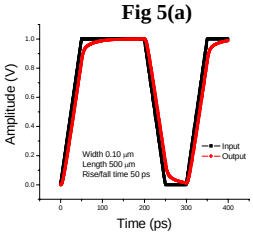

Fig 5(c)

Fig. 5 Input and output pulse shapes for a line width of 100 nm (wide-band model) with rise and fall time of (a) 10 ps, (b) 25 ps, and c) 50 ps

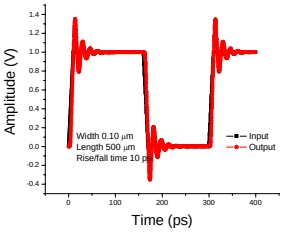

Fig 6(a)

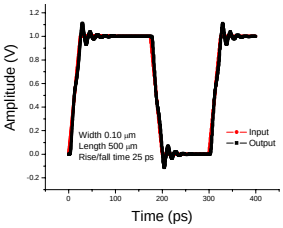

Fig 6(b)

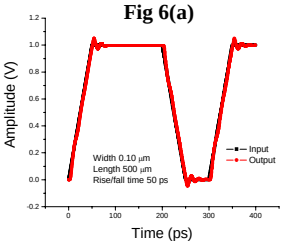

Fig 6(c)

Fig. 6 Input and output pulse shapes for a line width of 2 µm (wide-band model) with rise and fall time of (a) 10 ps, (b) 25 ps, and (c) 50 ps