Extended Abstracts of the 2006 International Conference on Solid State Devices and Materials, Yokohama, 2006, pp. 1012-1013

G-7-2

CuAl Alloy Interconnects as a Solution to the Trade-off between Reliability and Defect Density

T. Furusawa, D. Kodama, H. Miyazaki, M. Matsumoto, J. Izumitani, H. Matsumoto[1], S. Fukui, K. Hashimoto, S. Tawa, M. Okada, K. Tomita, Y. Nagaki[1], Y. Minoura[2], A. Ishii, N. Amou[1], K. Mori, K. Maekawa, N. Suzumura, K. Honda, Y. Hirose, and A. Osaki

Renesas Technology Corp., Itami, Hyogo 664-0005, Japan

Phone: +81-72-784-7362, E-mail: furusawa.takeshi@renesas.com

[1]Renesas Semiconductor Engineering Corp., [2]Ltec Corp.

Abstract

This paper describes the advantages of highly reliable Cu/low-k interconnects created by using a CuAl alloy seed. Post-CMP defect analysis shows, for the first time, that the CuAl drastically reduces both the density and the size of voids, thereby suppressing open failure. The reliability of SIV and EM also much improves, showing that the CuAl seed solves the trade-off between reliability and defect density observed in cases using a conventional pure-Cu seed and high-temperature post-ECP annealing.

1. Introduction

Stress-induced voiding (SIV) and electromigration (EM) failures are the most critical obstacles to achieving robust Cu/low-k interconnects especially when considering high-reliability device applications. When using a conventional pure-Cu seed, high-temperature annealing after ECP is known to be effective for improving the reliability. This annealing, however, causes voids in Cu, resulting in significant defect density [1,2].

In this paper, we present a solution to the trade-off: using a CuAl alloy seed. Defect density reduction by using CuAl is reported for the first time. SIV and EM reliability improvements are confirmed [3,4]. Further reliability improvement achieved by combining the CuAl seed with a sacrificial barrier metal process is also described.

2. Experimental Procedure

Interconnect test devices with 65nm-node dimensions were prepared as shown in Fig. 1. The defect density and the SIV and EM reliability were evaluated using the test devices. Both CuAl alloy and conventional pure-Cu were examined as seed layers for comparison. The vertical and horizontal distributions of Al in the CuAl alloy were analyzed by ICP optical emission spectroscopy (ICP-OES) and nano-SIMS, respectively.

3. Results and Discussion

Defect Density: For pure Cu, post-ECP annealing at high temperature results in significant defect density (Fig. 2). Most of the defects at the high temperature are large voids in comparison to the minimum interconnect width, potentially causing open failures. In the case with a CuAl alloy seed, in contrast, the defect density is less than 1/100 of that of the pure Cu. The void size is also reduced, showing that the density of fatal voids is drastically suppressed by using a CuAl alloy seed.

Al Distribution in CuAl Alloy: The vertical Al distributions evaluated by ICP-OES show that most of the Al remains near the seed even after annealing (Fig. 3). The horizontal Al distribution evaluated by nano-SIMS shows that, in ECP-Cu, the Al distributes only at grain boundaries (Fig. 4). This indicates that the Al diffuses from the seed to the ECP-Cu along the grain boundaries, and that this Al prevents Cu from diffusing during annealing, thus preventing void formation.

Reliability Test Results: The SIV test results showed that over 30% of the samples failed, even in the case with 2μm-wide interconnects, when using a pure Cu seed and high temperature annealing (Fig. 5). By using a CuAl alloy seed, SIV reliability improved greatly: 100% and 85% yields for 2μm-wide and 5μm-wide interconnects, respectively. The EM reliability was also much improved by using a CuAl alloy seed: over 7-times improvement in median time failure. Further improvement was achieved by using a sacrificial barrier metal process. The suppression of early mode failure results in an additional 3-times lifetime improvement at 0.01% cumulative failure.

4. Conclusion

A Cu/low-k interconnect using a CuAl alloy seed was shown to be a solution to the trade-off between reliability and defect density observed in cases using a pure-Cu seed and high-temperature post-ECP annealing. Post-CMP defect analysis showed that the CuAl alloy drastically reduces both the density and the size of voids, thereby suppressing open failure. The reliability of SIV and EM is also much improved by using the CuAl alloy seed. Further improvement in EM lifetime was achieved by using the sacrificial barrier metal process to suppress early mode failure.

References:

[1] S. Parikh et al., Proc. of IITC, p.183 (2001).

[2] G. B. Alers et al., Proc. of IRPS, p.350 (2001)

[3] Y. Matsubara et al., Symp. on VLSI Tech., p.127 (2003).

[4] K. Maekawa et al., Proc. of AMC, p.221 (2004)

[5] C. C. Yang et al., Proc. of IITC, p.135 (2005)

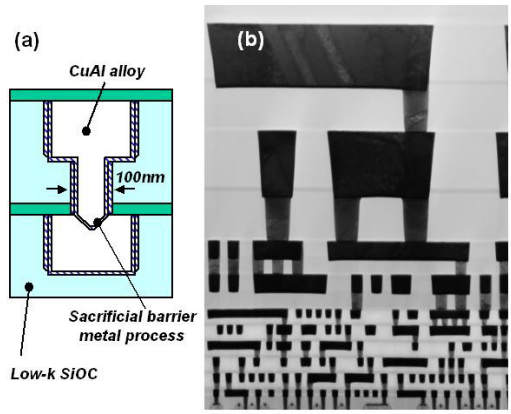

Fig. 1 Schematic of intermediate interconnect layers (a) and cross section of 65nm-node, 10-layer interconnect (b).

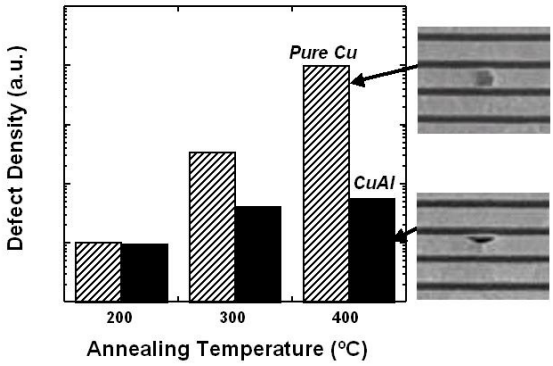

Fig. 2 Defect density comparison for pure Cu and CuAl alloy.

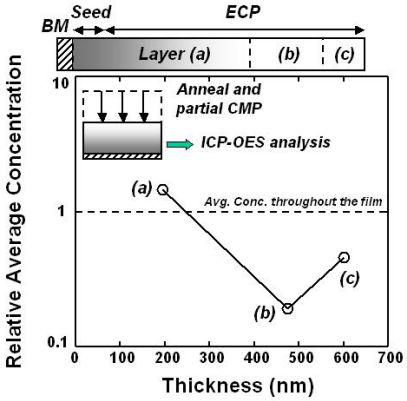

Fig. 3 Average Al concentrations for layers (a), (b) and (c) evaluated by ICP optical emission spectroscopy.

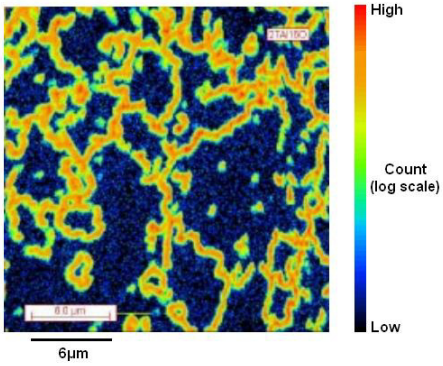

Fig. 4 Al distribution on annealed ECP-Cu surface evaluated by nano-SIMS.

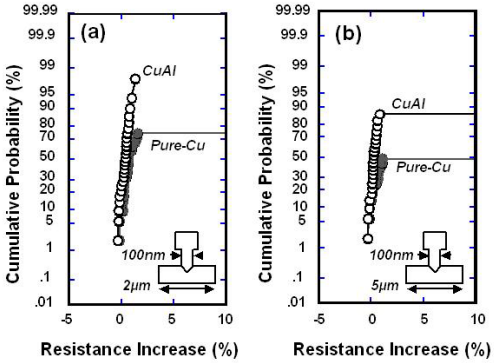

Fig. 5 Via-chain resistance increase after 1000-hour stress-induced voiding test at 200°C.

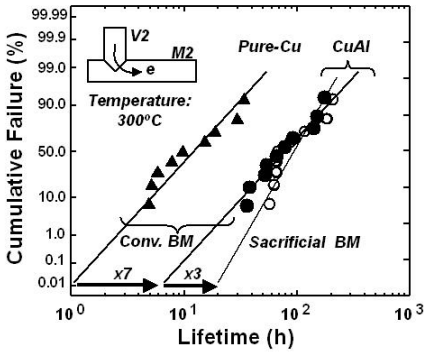

Fig. 6 Electromigration test results for 100nm-diameter vias.