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Challenges of Cu Metallizatioin for 45nm and beyond

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1. Introduction

Cu metallization technologies are facing challenges from the requirements of performance, reliability spec, and process capability as the interconnect geometry shrinks continuously. For interconnect performance, Cu resistivity rises up when the Cu line width is close to the mean free path of electron (450A) [1]. Surface scattering and grain boundary scattering need to be reduced to minimize the increasing of resistivity. For reliability spec, the reduction of geometry to carry same current poses increasing of current density requirement. For process capability, better coverage of barrier/seed and better gap filling ECP capability are required to reach void free gap filling.

This paper will address Cu metallization challenges raised by feature size diminution in terms of gap filling, electron scattering reduction, and reliability enhancement. New materials and new technologies aiming to fulfill these requirements for future generation process are discussed.

2. Challenges of Gap Filling by Feature Size Shrinkage

Fig.1 shows the feature size shrinkage as a function of generation. The ohmic drop within the feature becomes very severe as Cu seed layer thinning is required for nano-scale feature void-free filling. Fig. 2 shows the schematic diagram of the ohmic drop in the feature associated with non-conformal thin PVD Cu seed layer. New chemical that induces stronger electrolyte charge transfer resistance is required to achieve void-free gap fill. Cu ECD void-free gap filling can be achieved through tuning additive components in the electrolyte with appropriate plating currents [2]. However, depending on the pattern density, the additive adsorption (denoted as) could be very different. Fig.3 shows that iso and dense patterns have different plating current requirements for void-free gap filling. Through appropriate tuning of plating current, uniform bottom-up void-free gap filling can be achieved.

An alternative approach for better gap filling is to improve the conformality of the seed. Non-conformality PVD thin seed can be avoided by direct plating on barrier [3,4]. Fig. 4 shows cross-sectional TEM step coverage of EG Cu seed layer within a 0.06 um-wide trench. A continuous electro-grafted Cu layer with uniform thickness of 8 nm is formed at both sidewall and bottom. The profile of post EG seed has a much lower aspect ratio than that of PVD seed, which is friendlier for ECD gap filling. Lower Rs with tight distribution was obtained with EG Cu seed process due to void-free trench filling (Fig 5). With new additive and direct plating technology, conventional ECD process could be further extended beyond 45 nm generations.

3. Driving for High Electromigration Resistance

Fig. 6 shows Electromigration (EM) current density requirements of each generations as summarized by the ITRS 2004, which predicts that a 2X increase from generation to generation. SiC or SiCN are the most adopted Cu top capping material. The Cu top interface with SiCN was reported as the primary diffusion path during EM stress. To meet 45nm or 32nm EM requirements, new approaches to improve the Cu top surface adhesion is necessity. A self-aligned CuSix formation by thermally treat Cu in SiH4 based ambient is one alternative to improve Cu top surface adhesion.[5] Selective CoWP caps formed by means of electroless deposition have been reported to be effective Cu diffusional barriers with good adhesion to Cu and dielectric [6]. Fig 7 shows that 2x or 10X of EM improvement were demonstrated with CuSix or CoWP cap. For the CuSix capping layer, although its adhesion was improved, its SM failure rate was higher than conventional dielectric barrier, as shown in Fig. 8, and the degradation was hypothesized to result from the excessive vacancies generated by the introduction of silicon into Cu in the CuSix processing.

CoWP capping was found a promising approach to improve both EM and SM performance. However, due to intrinsic instability of the electroless deposition, controlling the selectivity is not straightforward. As illustrated in Fig. 9 that high line-to-line leakage induced by selectivity loss was observed with thicker Co depositions. To enhance the electroless Co selectivity, a surface treatment by chemical grafting (CG) prior to Co deposition was introduced [7]. The organic grafting precursors were designed to selectively chemisorb on the Cu surface to increase its chemical affinity to Co ions in the solution. Fig. 10 shows that with CG, the selectivity of Co capping was greatly improved..

5. Conclusions

The key challenges of Cu metallization for 45nm and beyond have been discussed. We have shown that through adequate control of chemical and process optimization, nano-scale void-free gap filling can be achieved. Direct electro-deposition was also demonstrated, which successfully extends the current ECD beyond 32nm generation. In addition, electroless CoWP is a promising material for EM and SIV performance. Controlling the selectivity of electroless Co cap layer is one of the major challenges to implement this technology.

Reference

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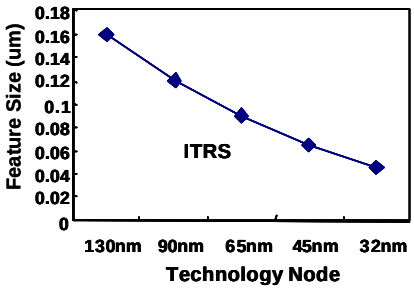

Fig.1 Challenges of void free gap fill increases with generations

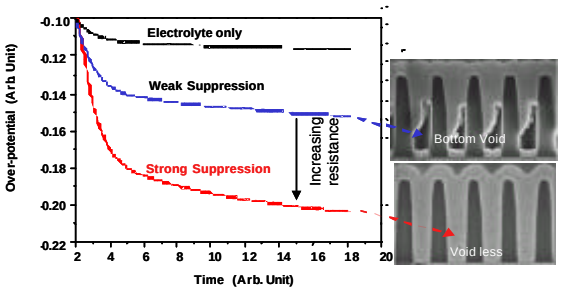

Fig.2 New additives for void free gap filling with thin seed

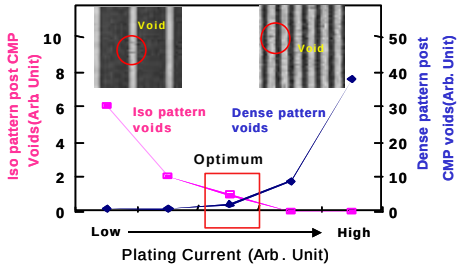

Fig.3 Optimization of platting process for iso/dense pattern void-free gap filling

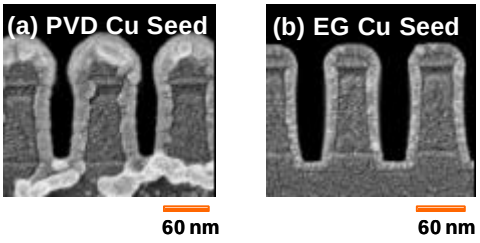

Fig.4 XSEM of 45nm-node trenches after (a) PVD and (b) EG seed

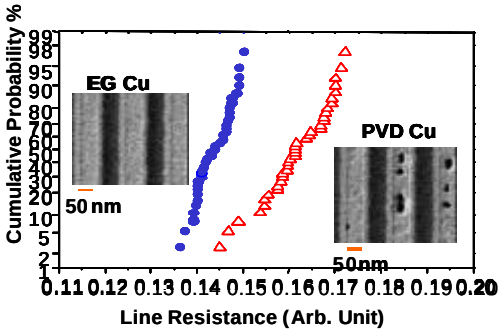

Fig.5 narrow line resistance of PVD and EG seed layers

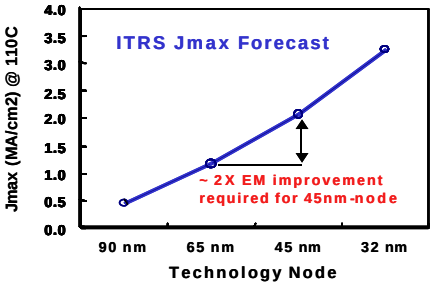

Fig.6 The requirements of EM Jmax increases with generations

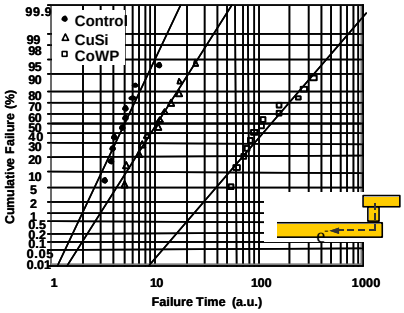

Fig.7 Effect of Cu cap processes on EM performance

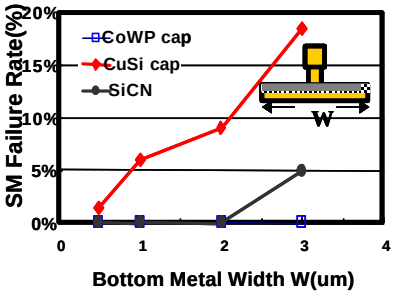

Fig.8 Effect of Cu cap processes on SM performance

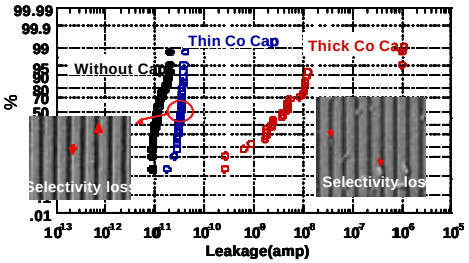

Fig. 9 Co cap thickness effect on selectivity loss

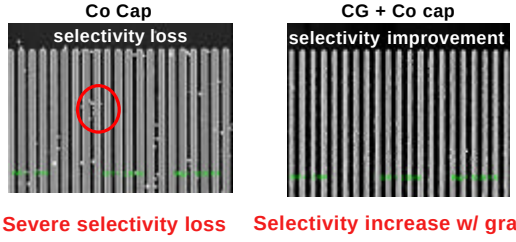

Fig. 10 Selectivity improvement by using chemical grafting process